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PROCEEDINGS OF SCIENCE

Fast data acquisition measurement system for plasma diagnostics using GEM detectors

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This work refers to currently being developed measurement system for plasma diagnostics for ITER-oriented tokamaks. For most of the GEM detector readout structures, large number of input channels is required to form the measurement system. This is especially important for two-dimensional GEM readout structures. Presented measurement system layout is a general model for further implementation. System is based on fast serial gigabit links and PCI-Express interface for communication. The system can support up to 512 measurement channels, per each PCI-Express x16 slot. The system consists of several modules – PCI-Express 8-to-1 switch, Analog Front End, ADC Front End, and FPGA backplane boards. Implemented data processing algorithms allow fast raw data acquisition and processing in real time. The integration algorithms allow measurement system to work with high rates from the GEM detector.

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1. Introduction

This work refers to the measurement system for plasma diagnostics for ITER-oriented tokamaks that is currently under development. In thermonuclear fusion research reactors (i.e. ITER), precise determination of the level and spacial distribution of the plasma soft X-ray radiation will be important for plasma parameters optimization. The system is based on the Gas Electron Multiplier (GEM) detector with high speed communication interfaces and effective algorithms for data processing, implemented in the FPGA units and in real time software [1]. The current implementation of hardware allows achievement of high signal rates from the detector. The system can work in two modes: First mode performs fast raw data acquisition of the analogue signals, giving therefore important information about the plasma or other radiation sources. Second mode calculates online charges registered on the GEM channel for further post processing done by software running on embedded PC. Due to modular structure of the measurement system, GEM detector readout boards can have different readout structures (1D, 2D, redundant, etc.). The system can work with one- or two- dimensional readout boards. Advanced gigabit serial communication interfaces are used in order to provide high throughput of the data to the post-processing algorithms. The main goal of the work was to develop a new generation of system with large number of measurements channel and high sampling speed.

2. GEM detector readout structures

Most commonly used GEM detector readout structures are one- and two- dimensional. One-dimensional readout boards are simpler for analysis in terms of position of the photons absorbed in the detector conversion layer. Therefore they require less channels and provide good spatial resolution. In terms of two-dimensional readout board, measurement systems require connection of twice or three times more signals from the readout board. The position and charge calculation algorithms are also much more complex [2]. However, this kind of structure (i.e. honeycomb pixels) is useful for the experiments with different intensity of radiation, i.e. plasma generated by the lasers. Complex readout structures of GEM detector require simultaneous, high-speed handling of large amount of channels by the measurement system [3].

3. Measurement system layout

The measurement system hardware model is divided into several parts. The description is based on 64 channels configuration of the system. The GEM detector's analog output channels (from readout board) are connected to the Analog-Frontend boards (AFE). The design is radiation-hard, allowing mounting of the units in different places, near high electromagnetic fields and in neutron flux. Boards contain preamplifier and shaper circuits, offset correction and fast comparators. Boards can also work in analog charge integration mode. The analog signals are transmitted to the ADC Frontend boards (ADCFE) using high speed differential cables.

Most important parts of the ADCFE boards are 12-bit ADCs. One ADCFE board can simultaneously acquire signal from 16 channels with 125 MHz sampling speed. ADCFE boards also communicate with integrated circuits on the AFE boards using serial communication links in LVDS standard. The ADCFE boards provide diagnostics of the hardware, i.e. current and temperature monitoring.

Digital samples of raw or integrated analog signals from the GEM detector, are transmitted to the FPGA backplane boards from the ADCFE boards using serial LVDS interfaces. On each FPGA backplane board up to 4 ADCFE boards can be mounted. Each FPGA backplane handles up to 64 measurement channels. Backplane board contains Artix7 FPGA as the main processing unit. FPGA firmware handles several functions, i.e.:

- Acquisition of the signals from the ADCs (from ADCFE boards)
- Data processing – charge integration, timestamps
- Data management – DDR3 memory data storage and control
- System configuration and monitoring – clock distribution and ADC initialization, offset calibration, temperatures and currents readout etc.
- Communication with the measurement system concentrator using PCI-Express links

The final position and energy calculations will be made in the embedded PC unit at post-processing stage. The backplane boards (FPGA units) are connected to the PC via data concentrator using PCI-Express communication links. Two configurations are available:

- Direct connection to the PC using mSAS – PCI-E adapter
- Connection through PCI-Express switch (data concentrator) 8-to-1 using mSAS cables

Fully populated system can work with 512 measurement channels (using one x16 GEN3 PCI-Express slot in the embedded PC), working with 125 MHz sampling speed for each channel [4][5]. Figure 1 presents readout section of the GEM measurement system, handling 64 measurement channels. The backplane board is connected to the PCI-Express switch mounted in the embedded PC.

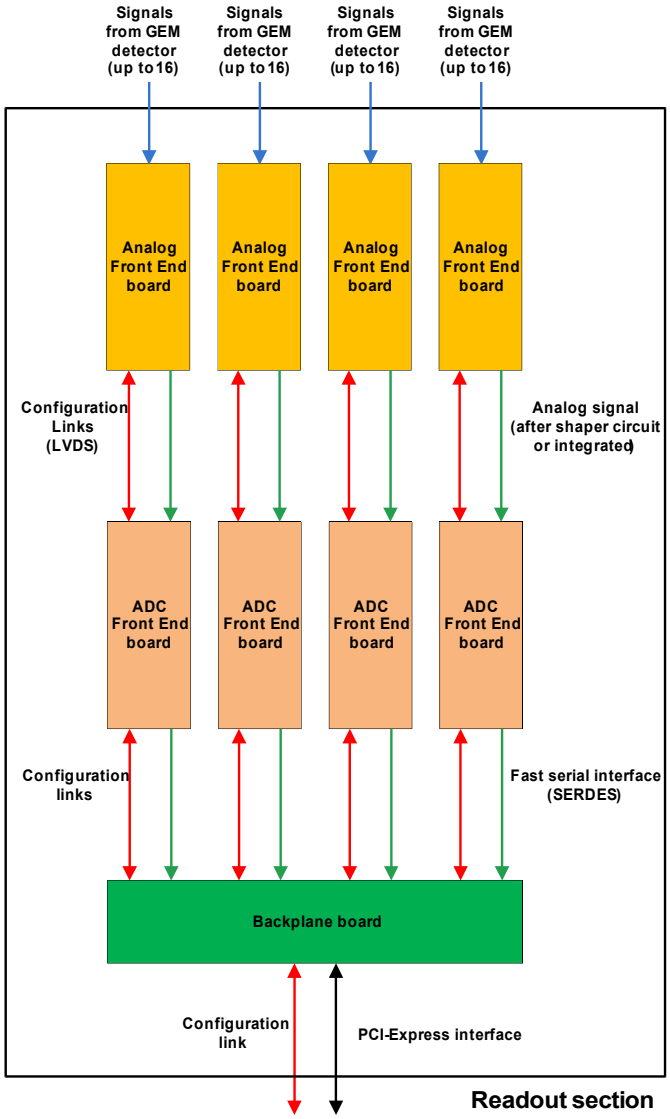

Figure 1 64-channels readout section of the GEM measurement system

4. FPGA firmware and implemented algorithms for fast data acquisition

FPGA firmware is the same for all of the FPGA units available on all the backplane boards. The firmware handles many different communication interfaces for startup configuration of the measurement system. Despite of the configuration part, several algorithms for the data processing were implemented [6]. Figure 2 presents main dataflow architecture for fast data acquisition, including:

- Long-time signal analyzers
- Fast signal recorder
- Fast digital charge integrator
- Test modes – digital pulse generator mode and counter mode

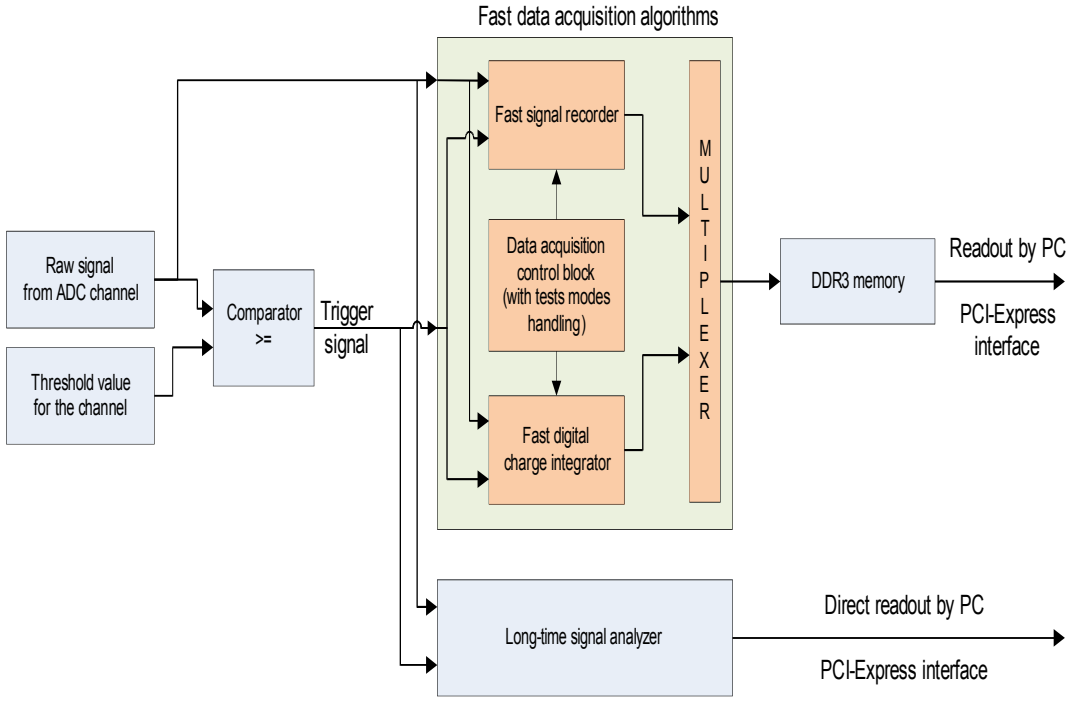

Figure 2 Fast data acquisition algorithms dataflow architecture implemented in the FPGA units

The output of the processing blocks can be connected to the serial streaming module, which automatically creates complex data structures with time markers. The data is then written in the DDR3 memory [7].

4.1 Long-time signal analyzers

The analyzers blocks allow registration of the analog, raw signal from the ADCs. Analyzers work as digital oscilloscopes with configurable trigger position (i.e. post-trigger), trigger edge, threshold level of the trigger, etc.. In one FPGA, 64 analyzers are implemented, one for each channel with 1024 samples memory. This mode is used for diagnostic purposes, i.e. can be used while adjusting the shaper circuits on the AFE boards. Analyzers work with 125 MHz sampling speed. Data is stored in the FPGA embedded memory blocks.

Trigger section works as analog comparator, with user-defined threshold levels for each channel. When trigger event occurs in one of the input channels, all signal analyzers start data acquisition at a same time. Figure 3 presents signal registered with long-time signal analyzers [5][6].

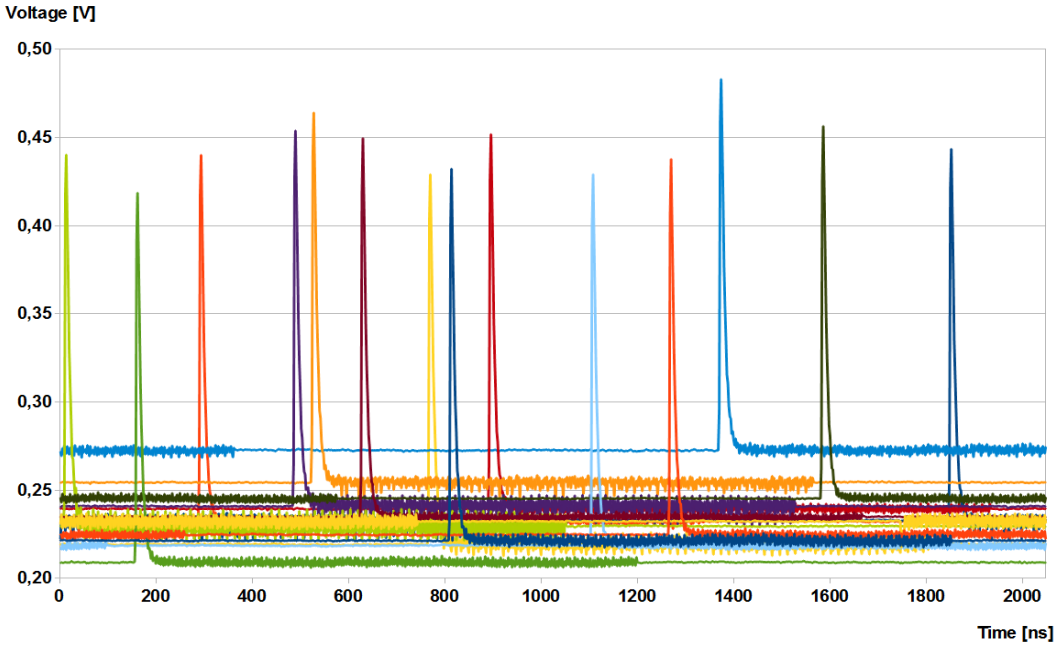

Figure 3 Raw analog signal acquired with the long-time signal analyzers (16 channels) [6]

4.2 Fast signal recorder

Fast signal recorders are available for each of the input channels (64 channels per backplane board). Signal is registered for 40 samples (one trigger event). All of the signal recorders start signal acquisition after trigger receiving, in the same way as long-time signal analyzers. Sampling speed is also of 125 MHz. After raw signal registration, the data is transferred to the DDR3 memory using special data flow manager. This mode allows fast acquisition of large number of photons in a short time. After registration of required number of samples, the embedded PC reads data from the DDR3 memory and performs offline processing – i.e. spectrum and photon position calculations. The data contains also timestamp with event number.

4.3 Fast digital charge integrator

Fast digital charge integrator performs online charge calculation from the raw ADC data. This significantly improves system throughput thanks to very short computation time of the charge and reduction of data transferred to the DDR3 memory. The algorithm after receiving the trigger starts integration of the raw signal. Independent algorithm measures average value of the input signal before the pulse. This constant value included in the charge value (integral) is subtracted at the end of the algorithm. Therefore no further computation of charge at post-processing stage is required. The charge data with timestamp information is stored in the DDR3 memory. An offline algorithm on the embedded PC can reconstruct position and spectrums for

user configurable number of energy bins. Fast digital charge integrator works with 125 MHz sampling speed. The details of the system are described in [5][4].

5. Measurement system control software

The system is controlled from the embedded PC using FCS (FPGA Configuration Software) [8]. FCS allows flexible configuration of large measurement systems, independently from the communication interface used in the system. In order to meet requirements of the complex measurement systems, FCS allows many settings of the system to be user-configurable. The system can be easily setup after boot and then configured under user needs with command line tools [9]. It also allows easy integration with graphical user interfaces. For the GEM measurement system, FCS uses PCI-Express [10][11] and USB interfaces for system configuration. FCS configures all of the integrated circuits available in the system including: AFE, backplane and PCI data concentrator. Then it does training of fast, serial links of ADCs . After system is set-up, user can configure it in different ways, including:

- Threshold levels for ADC channels
- Offset configuration
- Algorithms configuration (record length, test modes etc.)
- System status readout
- Download of measurement data from the DDR3 or FPGA memory

FCS is also used for system diagnostics, including temperature and voltage measurements.

6. Summary

The work presented in this paper was based on Authors previous experience in development of measurements system for tokamak facilities [12][13]. Significant upgrade was made in term of reworked construction of the previous system – dividing it to AFE, ADCFE, and backplane boards, in tree-like structure. The sampling speed is also higher, with improved charge integration time. Due to dividing AFE into separate modules with radiation-hard integrated circuits and proper shielding, the system can work in environment with strong electromagnetic fields and ionizing radiation. The implemented algorithms allow fast and efficient signals processing. Charge integration takes around 200ns, what enables to work with high rates from the GEM detector. FCS handles startup of the system and provides easy interface for user configuration. The measurement system can work with large number of readout channels from GEM detectors.

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