EFDA–JET–PR(13)11

D.F. Valcárcel, D. Alves, P. Card, B.B. Carvalho, S. Devaux, R. Felton, A. Goodyear, P.J. Lomas, F. Maviglia, P. McCullen, C. Reux, F. Rimini, A. Stephen, L. Zabeo, K-D. Zastrow and JET EFDA Contributors

The JET Real-Time Plasma-Wall Load Monitoring System

The JET Real-Time Plasma-Wall Load Monitoring System

D.F. Valcárcel[1], D. Alves[1], P. Card[2], B.B. Carvalho[1], S. Devaux[3], R. Felton[2], A. Goodyear[2], P.J. Lomas[2], F. Maviglia[4], P. McCullen[2], C. Reux[5], F. Rimini[2], A. Stephen[2], L. Zabeo[6], K-D. Zastrow[2] and JET EFDA Contributors*

JET-EFDA, Culham Science Centre, OX14 3DB, Abingdon, UK

1Associação EURATOM/IST, Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico, Universidade Técnica de Lisboa, P-1049-001, Lisboa, Portugal
[2]EURATOM-CCFE Fusion Association, Culham Science Centre, OX14 3DB, Abingdon, OXON, UK
[3]Max-Planck-Institut für Plasmaphysik, EURATOM-Assoziation, D-85748 Garching, Germany
[4]Associazione EURATOM-ENEA-CREATE, Univ. di Napoli Federico II, Via Claudio 21, 80125, Napoli, Italy
[5]Ecole Polytechnique, LPP, CNRS UMR 7648, 91128 Palaiseau, France
[6]ITER Organization, Route de Vinon sur Verdon, 13115 St. Paul Lez Durance, France
** See annex of F. Romanelli et al, "Overview of JET Results", (24th IAEA Fusion Energy Conference, San Diego, USA (2012)).*

Preprint of Paper to be submitted for publication in
Fusion Engineering and Design

ABSTRACT

In the past, the Joint European Torus (JET) has operated with a first-wall composed of Carbon Fibre Composite (CFC) tiles. The thermal properties of the wall were monitored in real-time during plasma operations by the WALLS system. This software routinely performed model-based thermal calculations of the divertor and Inner Wall Guard Limiter (IWGL) tiles calculating bulk temperatures and strike-point positions as well as raising alarms when these were beyond operational limits.

Operation with the new ITER-like wall presents a whole new set of challenges regarding machine protection. One example relates to the new beryllium limiter tiles with a melting point of 1278^{o}C, which can be achieved during a plasma discharge well before the bulk temperature rises to this value. This requires new and accurate power deposition and thermal diffusion models.

New systems were deployed for safe operation with the new wall: the Real-Time Protection Sequencer (RTPS) and the Vessel Thermal Map (VTM). The former allows for a coordinated stop of the pulse and the latter uses the surface temperature map, measured by Infra-Red (IR) cameras, to raise alarms in case of hot-spots. Integration of WALLS with these systems is required as RTPS responds to raised alarms and VTM, the primary protection system for the ITER-like wall, can use WALLS as a vessel temperature provider.

This paper presents the engineering design, implementation and results of WALLS towards D-T operation, where it will act as a primary protection system when the IR cameras are blinded by the fusion reaction neutrons. The first operational results, with emphasis on its performance, are also presented.

1. INTRODUCTION

1.1. THE ITER-LIKE WALL

The Joint European Torus (JET) has a new all-metal wall [1] with a beryllium main chamber and a tungsten divertor, similar to the wall that the International Thermonuclear Experimental Reactor (ITER) will have and thus named the ITER-like wall. The tile design was optimised for representative plasma equilibria and, as such, exhibits features aimed to improve power handling. The beryllium limiter tiles were designed to have a good power distribution over the tile surface and thus minimise heating. They are also castellated, to minimise the thermal stress due to heat expansion, and segmented to minimise the eddy currents. Each castellation is chamfered to shadow the gap between them and avoid the penetration of power into the tiles. Most of the divertor tiles are tungsten-coated Carbon Fibre Composite (CFC) tiles. These are not castellated but are chamfered to shadow the gap between tiles and avoid exposing it to high power loads. A single solid tungsten tile is installed made of lamellas to minimise eddy currents and each lamella is chamfered to shadow the gaps.

For the beryllium tiles a 950^{o}C surface temperature limit is set to avoid reaching the melting point of 1278^{o}C [2]. A pulse with a cold start of 200^{o}C, such as those at the beginning of the day, allows for a large temperature excursion. During a sequence of consecutive pulses, the tiles' starting

temperature builds-up thus gradually increasing the restrictions on power deposition for operation within the specified limits. When a beryllium tile is subjected to conditions that lead to the surface overheating it will melt and form droplets.

Defects on the tungsten-coated CFC can appear if the surface temperature goes above 1600^{o}C [2] and the difference in thermal expansion coefficients can enhance the formation of cracks in the tungsten coating. Apart from degrading the tile this can also lead to tungsten influx into the plasma followed by a possible disruption.

The solid tungsten tile was designed to suppress eddy currents and to withstand high thermal loads, as it is placed where the plasma outer strike-point is expected to be during most of the time. Despite the optimised design it will still melt if subjected to high temperatures. For these reasons the Plasma Facing Components (PFC) require monitoring during the experiments and the plasma pulse needs to be terminated, in a controlled way, if the measured temperatures are above the prescribed limits for operation.

1.2. WALLS DESCRIPTION

Cameras are the most suitable instrumentation for monitoring the surface temperature of the PFCs. The imaging sensors of the JET cameras are analogue monochrome Charge Coupled Device (CCD) cameras (HITACHI KP/M1AP), equipped with near infra-red filters [3]. These cameras are very reliable in the JET environment and in particular they do not require magnetic shielding. The downside of the choice of a CCD sensor is the sensitivity to neutron-induced background noise and damage [4]. The charged alpha particles, that result of the fusion reactions, are confined by the magnetic field. However the neutrons also produced are not and ultimately will deposit their energy on the PFCs or the cameras. When the latter occurs the temperature measurements are not reliable and the neutron fluence may be such as to blind the cameras. For this reason it is useful to have a complementary system, that is not influenced by the energetic neutrons, to take over the camera protection when necessary.

WALLS [5] is a system designed to monitor the first-wall using a model-based approach that does not rely on camera measurements. In the 1990s it was implemented in Texas Instruments' C40 Digital Signal Processors (DSP) and later the 2005 version (WALLS 2005) was developed using Versa Module Eurocard (VME) and Motorola PowerPC technologies. Its purpose was to monitor the JET carbon wall but it is insufficient for monitoring the new ITER-like wall. It does not provide an appropriate shadowing model for the power density deposition calculation on the limiter, neither a surface temperature model [6] and the number of tiles to monitor requires a volume of calculations that exceeds the capabilities of the WALLS 2005 hardware. The ITER-like wall requires monitoring of a large number of tiles. For each tile the surface or bulk temperature is required to be calculated as well as its distance to the plasma boundary (gap). In addition, for the divertor the position of the strike points is monitored to avoid that any of them moves to forbidden zones. When any of the machine's operational limit is exceeded WALLS raises an alarm.

Modern general purpose Central Processing Units (CPU) are devices that operate at high clock frequencies and contain several computing cores in a single chip. In particular multi-core CPUs based on x86 technology have been used in recent years in monitoring and control applications [7, 8, 9] and are appropriate options to consider for WALLS.

The Pulse Termination Network (PTN) [10] was deployed for collecting alarms from different plant systems with the purpose of terminating a plasma discharge in the most suitable way. The PTN has limited capabilities, in particular in terms of configurable plasma shut-down. The systems connected to the PTN receive a stop signal when key systems fail, or protection signals go off-limits, and these trigger a pre-defined sequence for the pulse termination independent of the pulse phase.

For the purpose of protecting the ITER-like wall several systems that monitor the wall and stop the pulse in a coordinated manner have been developed within the scope of the Protection of the ITER-like Wall (PIW) project. One of relevance is the Vessel Temperature Map (VTM) [11]. It receives the surface temperatures measured by the cameras for each defined Region Of Interest (ROI) and, based on the implemented logic, raises an alarm if the temperatures fall beyond the operational limits. The system that receives alarms from several sources and coordinates the stops is the Real-Time Protection Sequencer (RTPS) [12]. Should an overheat arise RTPS coordinates all the systems to take the appropriate measures to counteract the overheating.

This paper presents the design and implementation of WALLS for the protection of the ILW and its integration in the JET COntrol and Data Acquisition System (CODAS). Section 2 presents the essential physical ideas behind WALLS. Section 3 presents their design and implementation. WALLS has been running during the 2011 and 2012 campaigns, it was commissioned and some operational results obtained are shown in Section 4. The final part of this paper presents some remarks regarding this work as well as the future line of work.

2. THE WALLS PHYSICS BASIS

The thermal monitoring of the first-wall requires the surface temperature calculation of the limiter tiles and the bulk energy of the divertor tiles. The former is required to monitor the beryllium tiles that can reach melting temperature at the surface and the latter allows to protect both the divertor tiles and supporting structures. These calculations rely on the determination of the power that exhausts the plasma and on a model on how it propagates to the tiles. Once the power on the tile surface is known the surface temperature or bulk energy can be determined. For the divertor tiles the field line inclination angle $\theta_{\perp}$ with respect to the tile surface is also monitored to minimise the power deposition in the gap between tiles. For the thermal models it may be useful to determine some parameter values as a function of the plasma confinement mode, so the model for the real-time confinement mode determination in WALLS is explained. The cylindrical coordinate system (r, ϕ, z) is used throughout this paper. ϕ refers to the toroidal direction, whereas r and z are the radial and vertical coordinates respectively.

A fusion plasma starts by being ohmically heated but this process loses efficiency at higher

temperatures. JET uses Neutral Beam Injection (NBI), Ion Cyclotron Radiation Heating (ICRH) and Lower Hybrid Current Drive (LHCD) as auxiliary methods to heat the plasma or drive current.

A part of the power that is injected into the plasma, P_{ohm} plus P_{heat}, is lost by radiation, P_{rad}, and it can be measured by a bolometer diagnostic. Another is stored in the plasma, $^{dW}/_{dt}$, and the remainder, P_{exh}, is accounted for as the transport of particles escaping through the boundary. This is shown as a power balance:

$$P_{ohm} + P_{heat} = P_{exh} + \frac{dW}{dt} + P_{rad} \tag{1}$$

$$P_{ohm} = - \frac{d\Psi_b}{dt} I_p - \frac{d}{dt}\left(\frac{1}{4}\mu_0 R_0 l_i I_p^2\right) \tag{2}$$

The first term is related to the loop voltage $V_{loop} = - \frac{d\Psi_b}{dt}$ and the second the magnetic energy stored in the plasma taking into account the normalised internal inductance l_i. R_0 is the tokamak major radius and μ_0 the magnetic permeability of vacuum.

The particles that exhaust the plasma escape into a region in the outside vicinity of the boundary, the Scrape-Off Layer (SOL), and move along the field lines until they deposit their energy onto a PFC with its subsequent heating. During this free path they undergo a cross-field diffusion process, although more constrained, and it is assumed that the power density distribution follows an exponential decay across magnetic surfaces [13]. The power density ultimately deposited at a point of a given surface depends on the angle with respect to the incident field line and on the local flux expansion. Finally taking into account the flow F in the direction of the surface the expression that allows to determine the power density Q at a point of the surface is:

$$Q(\Psi) = F \frac{P_{exh}}{2\pi\lambda_{mid} r_{mid}} \frac{B_\theta}{B\theta_{mid}} \frac{\sin\eta}{\sin\zeta} e^{-\frac{\Psi-\Psi_b}{2\pi r_{mid} B^\theta_{mid} \lambda_{mid}}} \tag{3}$$

This point is labelled in terms of its total flux Ψ to get independence regarding physical coordinates, where Ψ_b is the plasma boundary flux. λ_{mid}, r_{mid} and B^θ_{mid} are respectively the scrape-off length, the radial coordinate of the boundary and the poloidal magnetic induction field on the outboard midplane; B_θ is the local magnetic induction field at the point of calculation; $\zeta = \arctan \frac{B_\theta}{B_\phi}$ is the field line angle. η is the angle between the field line and the physical surface and B_ϕ is the component of **B** in the ϕ direction:

$$B_\phi = B_0 \frac{R_0}{r} \tag{4}$$

with B_0 the magnetic field at the major radius.

Equation 3 contains the power flow F as the first term and the second one is the power density at the plasma outboard midplane, translated into a power density local to the tile by the third term that takes into account flux expansion. The fourth term takes care of the angle between field line

and the surface. The final term relates to the exponential decay of the power density across field lines.

The total power on a toroidally continuous ring of N_{tiles}, each a surface with finite length between two points with total fluxes Ψ_1 and Ψ_2, can also be expressed as:

$$P(\Psi_1, \Psi_2) = \frac{F}{N_{tiles}} [P(\Psi_2) - P(\Psi_1)] \tag{5}$$

$$P(\Psi) = P_{exh}\left(1 - e^{-\frac{\Psi - \Psi_b}{2\pi r_{mid} B\theta_{mid} \lambda_{mid}}}\right) \tag{6}$$

When a field line intersects a limiter or divertor tile it will deposit a given energy. Tiles beyond will receive less energy. In general terms this is called shadowing. In particular if it occurs between limiter tiles it is denominated limiter-to-limiter shadowing, and between divertor tiles denominated divertor shadowing. As a consequence the power density or power deposited on a point or a surface is less than what is calculated from Eqs. 3 and 5 and this effect needs to be taken into account in the models.

The final components in the thermal calculation chain are the thermal models. The limiter tile models determine the surface temperature at the tile midpoint. As these are castellated the heat propagation can be assumed to be one dimensional over the tile depth. These models are a discrete implementation of the one dimensional heat equation:

$$T_0^{j+1} = T_0^j + \frac{K}{\rho c_p} \frac{\Delta t}{\Delta x^2} (T_1^j - T_0^j) + \frac{\Delta t}{\rho c_p} \frac{Q_{tile}^j}{\Delta x} \tag{7}$$

$$T_i^{j+1} = T_i^j + \frac{K}{\rho c_p} \frac{\Delta t}{\Delta x^2} (T_{i-1}^j - 2T_i^j + T_{i+1}^j) \tag{8}$$

$$T_{N-1}^{j+1} = T_{N-1}^j + \frac{K}{\rho c_p} \frac{\Delta t}{\Delta x^2} (T_{N-2}^j - T_{N-1}^j) \tag{9}$$

T^i_j represents the temperature at the point i of the grid and at time instant j, Q^j_{tile} is the power density at the tile surface, ρ the material density, K the heat conductivity and c_p the specific heat. Δx is the spacial resolution of a material slab divided into N elements and Δt is the temporal resolution. Equations. 7, 8 and 9 can be written in the general state-space form:

$$x^{j+1} = Ax^j + Bu^j \tag{10}$$

$$y^j = Cx^j + Du^j \tag{11}$$

where $x^j = [T^j_0\ T^j_1\ \ldots\ T^j_{N-1}]^T$ is the state vector, $u^j = [\ Q^j_{tile}\ 0\ \ldots\ 0]^T$ is the input vector and $y^j = [T^j_0\ 0\ \ldots\ 0]^T$ the output vector, all at time step j. The models for the divertor are similar but allow to calculate the bulk temperature and energy of the tiles from the total incident power (taking

into account divertor shadowing).

Another important definition is the $\theta_{\perp}$, an angle related to the wetted area of a tile and it is given by:

$$\theta_{\perp} = \arctan \frac{B_{\perp}}{B_{\phi}} \tag{12}$$

where $B_{\perp}$ is the component of **B** perpendicular to the surface of the tile.

Determining the plasma mode, L- or H-mode, in real-time allows to define different values for parameters that depend on it, such as the power density scrape-off length [13], and enables WALLS to be more flexible under different operational conditions. The automatic determination of the transition, albeit difficult, it is possible and machine learning methods have been applied [14]. It is known that when the injected auxiliary power exceeds a power threshold the plasma shows enhanced confinement, thus it is possible to devise scaling laws that relate the evolution of the power threshold with various plasma parameters.

The WALLS H-mode detection algorithm is based on such scaling laws, comparing the plasma exhaust power P_{exh} with the engineering scaling of the L-H threshold power P_{L-H}, determining that a lower dominant X-point plasma is likely to be in H- mode if $P_{exh} \geq P_{L-H}$. The used L-H power scaling is the ITPA2008 [15]:

$$P_{L-H} = 0.0488 \cdot n_{20}^{0.717} \cdot B_T^{0.803} \cdot S^{0.941} \tag{13}$$

In this expression n_{20} is the line averaged electron density ($\times 10^{20}$ m^{-2}), B_T is the vacuum toroidal field (Tesla) at $R_0 = 2.96$m and S is the plasma poloidal cross-sectional area (m^2).

Because the threshold scaling is derived from a statistical analysis of a large database, assembled from the major tokamaks, deviations of the actual L-H transition from the prediction are to be expected. In addition, these engineering scalings do not take into account several plasma physics factors that are known to influence the power necessary to trigger a transition into H-mode, such as the proximity of the X-point to the PFCs [16], the plasma current profile or the toroidal rotation. A criterion for transition into H-mode is:

$$\frac{P_{exh}}{P_{L-H}} \geq \eta \tag{14}$$

where η is a fraction to be determined empirically from operational data and it can assume different values according to the plasma configuration, limited (inner or outer contact point) or diverted (lower or upper dominant null).

3. DESIGN AND IMPLEMENTATION

3.1. REQUIREMENTS

WALLS performs a series of checks over the calculated physical parameters. The checks can be

grouped in datagram late arrival, geometric and thermal checks. This section deals with describing each of these groups along with other technical requirements for the WALLS system.

The Real-Time Data Network (RTDN) is a network, based on Asynchronous Transfer Mode (ATM) technology, used at JET to exchange data between real-time systems [17]. Data is transmitted in datagrams and the datagram late arrival checks consist of ensuring that WALLS does not miss required datagrams.

The set of geometric checks are the divertor strike-points position and $\theta_{\perp}$, the High-Field Gap Closure (HFGC) tile $\theta_{\perp}$ limit above a given power density threshold and the main chamber wall minimum gap limit above a given power exhaust threshold.

The divertor strike-points checks ensure that they do not cross to forbidden regions and do not expose the area between tiles to excessive power loads. The HFGC tile $\theta_{\perp}$ limit above a certain power threshold limits the power deposited on this tile, that it is not meant to receive more than a modest power load. The main chamber wall minimum gap limit provides a simple protection scheme that, when above a predefined power exhaust, ensures a sufficient clearance to the beryllium tiles.

The set of thermal properties to monitor are the limiter tiles surface temperature, both on the inner and outer walls, and the divertor tiles bulk temperature and energy.

The limiter tiles surface temperature limit ensures plasma operation below the melting temperature of beryllium. The divertor tiles bulk temperature monitoring allows operation of the tungsten coated CFC tiles within their temperature limits and the energy monitoring ensures the integrity of their supporting springs.

The limiters required to be monitored are the Inner Wall Guard Limiter (IWGL) on the inner wall and the Wide Outer Poloidal Limiter (WOPL) on the outer wall. Provisions must be made to accommodate two more limiters on the outer wall, the Narrow Outer Poloidal Limiter (NOPL) and the ITER-Like Antenna Outer Poloidal Limiter (ILAOPL). This means that the number of tiles to monitor on each limiter are 19 for IWGL, 25 forWOPL, 25 for NOPL and 18 for ILAOPL, totalling 87 tiles. The divertor is composed of 7 tungsten-coated CFC tiles and 1 solid-tungsten tile.

The plasma confinement mode detector is required for the real-time determination of the scrape-off length.

WALLS is required to run on a 10ms cycle time, an interval short enough for protection at the time scale of the plasma movements and thermal inertia, and at the same time long enough to accommodate all the required calculations. Also each alarm is to be raised only if the limits are exceeded over an assertion time of 50ms.

Finally it is required to be designed in a modular and extensible way, so that in the future new modules or monitoring of extra tiles can be added, and to integrate into the JET CODAS.

3.2. HARDWARE AND SOFTWARE

The software framework selected for the development of WALLS was BaseLib2 with the Multithreaded Application Real-Time executor (MARTe) framework [18]. These are C++ libraries,

tailored for the real-time execution of code, that were already ported to several Operating Systems (OS), including VxWorks, Linux with Real-Time Application Interface (RTAI) and Linux with real-time extensions. MARTe is a modular framework where code is organised in independent Generic Application Modules (GAM) that exchange data via a Dynamic Data Buer (DDB) and are executed sequentially in real-time threads. A MARTe application may contain one or more realtime threads and the execution of each is triggered periodically by a clock source. The performance and reliability of BaseLib2 and MARTe were already demonstrated in several fusion experiments in Europe [9? , 19, 20], in particular at JET [12, 18, 21].

Several Commercial Off-The-Shelf (COTS) hardware and software combinations, shown in Table 1, were considered for WALLS, mainly due to high availability and with existing versions of BaseLib2 and MARTe. Two of them are based on a combination of VME hardware and a single-core PowerPC CPU running the VxWorks real-time OS. The other two on a COTS Personal Computer (PC) with multi-core x86 technology running the Linux OS with real-time extensions.

To determine the most appropriate option the performance of the various choices was assessed by repeatedly running a state-space representation of a 1-D thermal diffusion model. The execution time of the model was measured statistically over a large number of cycles. For the time measurements the internal timer of each system was used through the Application Programming Interface (API) exposed by each operating system and the selected software framework used in the tests was BaseLib2/MARTe.

Table 2 shows the results observed for the execution time on each option. For each of them the execution time gets smaller as the processor frequency increases, the AMD and Intel based platforms exhibiting the best performance in terms of execution time, but the MVME 5500 system exhibiting the best overall jitter (in percentage). Table 2 also shows the cycle time measured in each of the systems. On all systems the measured cycle time is the expected 10ms, but the AMD x86 system shows the lowest overall jitter.

Table 3 presents a summary of the adopted hardware and software solutions. The AMD x86 was selected due to high availability on site, the best measured performance and the less cumbersome software development cycle under Linux versus the same cycle under VxWorks. This table also shows the BIOS options that were disabled and Linux kernel parameter set to increase the performance and the determinism in the code execution (see [21] for more on this subject).

Although the performance of the AMD CPU allows already the execution of more models in the same cycle than the PowerPC, the presence of several processing cores enables the possibility of expanding WALLS in the future.

3.3. DESIGN

Figure 1 shows the WALLS integration in the context of the JET CODAS environment. The integration is accomplished via the RTDN and Ethernet. The ethernet links use a module called CODASLib [22] that implements the JET proprietary client-server CSL8 protocol over Transmission

Control Protocol (TCP)-based communication.

During a pulse, JET transitions between different states and each real-time system must behave in accordance with the present state. The supervisory system drives the WALLS' state machine, shown in Fig.2, by sending event messages. If MARTe issues an error during a state change it is shown on the JET mimics displays.

Level-1 provides the user interface to configure MARTe, allowing to set limits and physical parameters. On the RTPS side it provides the configuration of responses to alarms.

The data recorded by the real-time systems is stored after the pulse in a JET Pulse File (JPF). The General Acquisition Program (GAP) requests the signals and stores them in database. WALLS records over 1800 signals during the pulse. After the pulse these are available to reconstruct the sequence of events that occurred and to diagnose any problem in WALLS.

MARTe also makes available logging capabilities and HTTP introspection. The first allows each module to log activity messages in a server. The latter is a facility that enables the user to introspect the modules using a web browser.

Figure 3 puts WALLS into the RTDN context showing the dependency between WALLS and other real-time systems.

WALLS receives datagrams from the required diagnostics: the toroidal field circuit current measured by Shape Controller (SC); magnetics measurements; the plasma internal kinetic power and cross-sectional area calculated by BetaLi [7, 23], also a MARTe-based system; the total power emitted by NBI, RF and LH; the power lost by radiation; and temperature measurements from thermocouples. The Real Time General Services-Protection (RTGS-P) system transmits two useful datagrams, a timing datagram and the line averaged density measurement on a second datagram.

WALLS sends a datagram with calculated physical quantities to VTM, to the Real-Time Pulse Protection (RTPP) and to the Real-Time Central Controller (RTCC). The integration with RTPP and RTCC enables the JET users to experiment with algorithms for machine protection (RTPP) and plasma control (RTCC).

WALLS sends an alarms' datagram to RTPS. The RTPS configuration determines the appropriate actions for each alarm. If the communication between these systems is broken and RTPS does not receive a given number of consecutive datagrams from WALLS it may stop the pulse.

Figure 4 shows the WALLS data flow that implements the project requirements. The modules can be grouped into several main groups: RTDN inputs, waveform generators, data processing modules, checks, RTDN outputs and data collection.

The WALLS data flow can generate a high volume of calculations to be performed. This strongly affects the design within the context of MARTe and it had to be considered from the beginning of the design process. A typical MARTe application uses a single real-time thread for a linear and cyclic execution of processing modules. This means that for a given hardware there is a limit on how many modules can be executed in a single real-time thread in the prescribed cycle time.
Several options were considered to address this issue. The option of using the available cores in

modern multi-core CPUs to parallelise the processing over several execution modules is the most promising one, as it allows to make use of all the processing power available in a single processor. The library developed for this purpose was presented at [24] and it consists in splitting the operations into smaller tasks that can be executed concurrently by each core, adding them to a queue and having worker threads that fetch work from the queue and execute it. This approach has several advantages: the data flow is kept organised in a single MARTe real-time thread, the load balance is automatic and the tasks are small enough so the load balance is closer to the optimum performance.

The MARTe real-time thread executes periodically and for that it needs to synchronise to a time source. For WALLS the chosen time source is a special RTDN datagram transmitted once every 2ms by the RTGS-P system. This process is shown in Fig.5. The timing for all systems is generated by the JET Central Timing and Triggering System (CTTS). RTGS-P samples the CTTS and generates a datagram every 2ms with this information. The datagram is received by the ATM low-level driver, passed to the MARTe ATM high-level driver and finally to the Time Triggering Service (TTS) module. The TTS counts the number of datagrams received and when the count is a multiple of 5, for a 10ms cycle time, it triggers the execution of the real-time thread.

3.4. IMPLEMENTATION

The present section describes the implementation of each WALLS' module, for the physics calculations and the alarm logic.

3.4.1. Magnetic reconstruction

The XLOC reconstruction algorithm [25] has been in use at JET for the real-time determination of the flux map and information about the plasma from magnetic measurements. To facilitate this task Felix [26] is the real-time package that allows to extract information from the flux map obtained using XLOC coupled with enhancements [27]. A tailored configuration was developed to determine the information required by WALLS.

The Felix model reconstructs the magnetic flux on 5 regions using a subset of the magnetic measurements for each. The flux map allows to retrieve information, based on the flux and magnetic field, regarding the plasma. Firstly, the upper and lower X-point and the plasma contact point positions are searched. With this information known the boundary flux, gaps and strike-point positions can be determined. WALLS determines the standard JET gaps [28], mainly for validation of the flux map

with SC, but these are available also for checks: Radial Outer Gap (ROG), Radial Inner Gap (RIG), and 5 TOp Gaps (TOG). WALLS also determines one gap normal to each tile's midpoint that is used to guarantee a minimum clearance to the wall.

Several strike-point definitions exist to determine their position on both the divertor and the UDP. WALLS determines these again for validation against SC and checks. The strike-point definitions used at JET for control purposes are: Radial Strike Inner (RSI), Radial Strike Outer (RSO), Vertical

Strike Inner (ZSI), Vertical Strike Outer (ZSO), Upper Strike Inner (USI), Upper Strike Outer (USO), Upper Radial Strike Inner (URSI), Tungsten Load Bearing Septum Replacement Plate (WLBSRP) and Load Bearing Septum Replacement Plate (LBSRP).

WALLS determines on which divertor tile face the strike-points are using the Tile Strike Inner (TSI) and Tile Strike Outer (TSO) definitions which cover the entire divertor. A similar definition exists for the UDP and their names are Upper Tile Strike Inner (UTSI) and Upper Tile Strike Outer (UTSO). If UTSI and UTSO are successfully determined, then UDP is acting as an upper divertor, otherwise it is considered a limiter. When TSI, TSO, UTSI and UTSO are determined then their position, B_r, B_z and B_ϕ are determined as well. Figure 6 shows the URSI strike-point definition that goes from the upper left almost to the middle part of the divertor. The signal generated is the radial coordinate of the leg intersecting these line segments.

The final task of Felix is to calculate the flux and field at the midpoints of the limiter tiles and edges and midpoint of the divertor tiles to be used by the power calculation modules.

3.4.2. Toroidal field calculation

This module determines the toroidal field from Eq.4. It can receive two types of input signals, the toroidal field circuit current and the list of radial position signals where to calculate the toroidal field. If no signals for the radial positions are specified then a list of fixed radial coordinates list has to be specified in the configuration. The parameters specified in the configuration file are R_0, the number of coils N_{coils} and the number of windings on each coil $N_{windings}$. These parameters determine the factor K_0 that is used to calculate the field at R_0 from the circuit current I_ϕ, and it can be determined from:

$$B_0 = K_0 I_\phi \tag{15}$$

$$K_0 = \frac{\mu_0 N_{coils} N_{windings}}{2\pi R_0} \tag{16}$$

The output signals from this module are B_0 and an extra one for each field calculated at the specified positions.

3.4.3. $\theta_\perp$ calculation

This module calculates $\theta_\perp$ given by Eq. 12. The configuration of the module takes a set of normal vectors used to determine $B_\perp$ from B_r and B_z.

As input signals, it receives the magnetic field components and an index signal that selects which of the normal vector on the set to use. This latter feature is useful if the set of normal vectors refers to a complex structure, such as the divertor, and the index selects a tile face.

As output signals, the module produces the $\theta_\perp$ signal. This module is able to process $\theta_\perp$ for several field lines using the same set of normal vectors.

3.4.4. Plasma exhaust calculation

The plasma exhaust calculation module implements the evaluation of Eq.1 and Fig.7 shows its internal details.

The ohmic power component of the total exhaust power can either be produced by this module or externally, in a different WALLS module or received via the RTDN. This module calculates the ohmic power from V_{loop} and plasma current I_p measurement:

$$P_{ohm} = V_{loop} I_p \tag{17}$$

Alternatively if BetaLi is used as the P_{ohm} source for WALLS, via RTDN, it takes into account the full expression as in Eq.2.

The boundary flux derivative in Eqs.2 and 17 is accomplished by a Finite Impulse Response (FIR) filter with configurable coefficients. The final step in the WALLS ohmic power calculation is a further FIR filtering process with configurable coefficients to eliminate the high-frequency components introduced by the derivative.

The $^{dW}/_{dt}$ term is calculated by differentiation of the plasma energy provided externally to the module, again via a configurable FIR filter. The plasma energy is currently supplied by BetaLi via the RTDN.

The auxiliary power signals P_{NB}, P_{RF} and P_{LH} are obtained externally via the RTDN and published by their system's local managers.

P_{ohm}, P_{NB}, P_{RF}, P_{LH} and P_{plasma} are each multiplied by a factor, F_{ohm}, F_{NB}, F_{RF}, F_{LH} and F_{plasma} respectively, and summed together. These factors are specified in the configuration file and are typically used to exclude some power terms, a useful feature during commissioning. If a radiated power fraction f_{rad} is assumed then $1 - f_{rad}$ is taken out of the sum, otherwise $F_{rad}P_{rad}$ is subtracted from the sum and this result is P_{exh}.

3.4.5. Plasma configuration and confinement mode calculation

From the boundary signals that Felix provides, the limiter contact point and the dominant X-point, this module generates an output signal whose value means the plasma boundary is undetermined (e.g. if there is no significant plasma current), limited, lower or upper diverted as specified on Table 4.

For the plasma confinement mode calculation Eq.13 is implemented in a general manner:

$$P_{L-H} = k \times \prod_i X_i^{y_i} \tag{18}$$

This enables the calculation of the L-H threshold power P_{L-H} for an arbitrary number of terms in the multiplication, each with its own exponent and a common coefficient. These are specified as parameters in the configuration file and the ITPA2008 configuration is currently in use with $k = 0.0488$, $X = \{n_{20}; B_0; S\}$ and $y = \{0.717; 0.803; 0.941\}$. The toroidal field is calculated internally

by WALLS, whereas the plasma cross section area is determined by BetaLi and the plasma line averaged density sent by RTGS-P. Once P_{L-H} is determined this value is compared with the calculated P_{exh}, using Eq. 14, and the plasma mode output signals is set as in Table 5. The value of η is specified in the configuration file and a default mode can be used to guarantee that the same scrape-off length is used while η is not tuned.

This module also outputs the scrape-off length for the current plasma mode. The possible values are specified in the configuration file but typically the L-mode value is twice the H-mode value.

3.4.6. Limiter power density calculation

To calculate the power density on the limiter tiles a model was developed taking into account limiter-to-limiter shadowing. This model is based on a simplified form of Eq.3:

$$Q(\Psi) = \frac{C_{tile}\, C_{coctr}\, P_{exh}}{tan\zeta}\, e^{-\frac{\Psi-\Psi_b}{2\pi r_{mid} B^{\theta}_{mid} \lambda_{mid}}} \tag{19}$$

C_{coctr} is the ratio between flows in opposite directions and C_{tile} is a pre-computed term, for the IWGL, WOPL and NOPL limiters, that takes into account shadowing, the scrape-off length and the geometry of the plasma and tiles [29]. This approach determines the worst power density that is possible to obtain on the tile and thus represents a conservative approach.

This module is a GAM that contains several power density calculation sub-modules and is responsible for initialising and preparing each one. The sub-modules implement the power density calculation model of Eq.19 and read the parameter C_{coctr} value, C_{tile} table and tile position R_{tile} and Z_{tile} from the configuration file. All the necessary physical quantities are read from the DDB as signals: P_{exh}; B_r, B_z and B_ϕ at the tile to determine tan ζ; r_{mid}, B^{θ}_{mid} at the outboard, machine midplane, boundary; λ_{mid} as output by the plasma mode determination module; and the fluxes Ψ at the tile and Ψ_b at the boundary. Each module outputs to the DDB the calculated power density at the tile and other signals for debug or visualisation purposes. These modules are prepared to use the WorkLibrary and can run in parallel if required.

3.4.7. Surface temperature calculation

The main module is a surface temperature calculation GAM that contains submodules, one per tile, to perform the surface temperature calculation using a 1-D thermal diffusion model in state-space representation. The GAM takes care of initialising and executing all submodules. Each of them is initialised from the thermal properties of beryllium and the geometrical properties of the tile. The properties are chosen offline to ensure stability. The surface temperature calculation GAM executes all submodules sequentially. It is also possible to run them in parallel via the WorkLibrary for an extra gain in performance.

During the real-time cycle each submodule reads a power density signal, performs the model calculations and writes a surface temperature signal. The matrix operations required for

the state-space model are optimised in case the matrices are zero, identity or diagonal. Prior to each pulse the model state is initialised from a set of temperature signals, one for each state. These signals can be constant signals to initialise the state from known values or dynamic readings from a measurement, such as thermocouples.

3.4.8. Divertor bulk temperature and energy calculation

For the divertor tungsten-coated CFC tiles the modules developed to calculate the bulk temperature and energy are shown in Fig.8. The plasma exhaust power P_{exh} is processed by the DivertorPowerPartition module and the outputs are the power on the inner P_{in} and outer P_{out} legs of the divertor configuration:

$$P_{in} = F_{in} \cdot P_{exh} \tag{20}$$

$$P_{out} = F_{out} \cdot P_{exh} \tag{21}$$

The two different fractions F_{in} and F_{out} are present to take into account the asymmetries in power flow in both divertor legs. These are obtained empirically and the power split is around $F_{in} = 0.3$ and $F_{out} = 0.7$.

P_{in} and P_{out} are then fed to the tile face power calculation module to determine the total power on each tile face i from Eq.5. For each tile face the module interpolates the flux quadratically along the face using the values at the edges, ψ_i^0 and ψ_i^1, and the midpoint ψ_i^m. The interpolation results in two fluxes, ψ_i^a and ψ_i^b, that are used to determine the total power. The other inputs required are the inner I_{in} and outer I_{out} strike-points index that indicate in what tile face the strike-points are at. P_{in}, P_{out}, I_{in}, I_{out}, ψ_i^a and ψ_i^b are used for the calculation of the total power on the tile face. These values, along with the total tile face power, are passed to the function that removes the shadowed power on that face. This takes into account the geometry of the divertor by processing the faces in the appropriate order (set in the configuration file) and keeping track of the flux values already accounted for. The result is the power on the entire toroidal ring and to get the individual tile face shadowed power it is necessary to divide by the number of ring tiles. The final step is performed by the implemented state-space models that read the power signals corresponding to the tiles' faces and output their bulk temperature and energy.

3.4.9. Conditional and logical modules

The set of modules to check conditions and raise alarms comprises four areas with distinct purposes: selecting limits, checking conditions, performing logical operations and applying hysteresis and aggregating logic signals.

The limit selection modules consist of two GAMs, the LimitSelectorGAM and the LimitSelectorWithInterpolationGAM. Both read a table of limits from the configuration file and receive a set of input signals that act as indices. The number of output signals is the same as index

input signals and the values are selected from the table based on the values on the indices. The names reflect the only difference between them in which the latter interpolates between table elements if the index is not in it, whereas the first returns a default value.

To check conditions the ConditionCheckGAM and TwoSignalConditionCheckGAM modules were developed. The ConditionCheckGAM contains one or more Comparison submodules whose purpose is to generate an output signal by comparing an input signal with a configured value. The comparison operation is set on the configuration file and can be chosen from the available operations $<$, $\leq$, $>$, $\geq$, $=$ and $\neq$. The Two Signal-ConditionCheckGAM compares two input signals with a configured comparison operation generating an output signal. The outputs of both GAMs are 32-bit integers that represent the logical value of the comparison, 0 if False and 1 if True. This type is used throughout all modules that handle logical signals.

It is useful to combine the result of several comparisons to generate a compound condition. For this purpose two logical operations were developed, the LogicAndGAM and the LogicOrGAM. Both receive an arbitrary number of logical input signals and the combined result of ANDing or ORing them is written as an output signal. Both GAMs inherit the common behaviour from LogicGAM and implement the specific operation in a pure virtual method. Other logical operators may be implemented in a straightforward manner.

Figure 9 shows the remaining modules in this set. A hysteresis module, named LogicHysteresisGAM shown in Fig.9a, was developed to ensure that spurious alarms are not set, e.g. due to a transient movement of the plasma when close to a limit. This GAM reads an arbitrary number of logical input signals and produces an equal number of output signals. For any input signal, when it transitions from 0 to 1 the number of cycles it stays at 1 is counted and if it exceeds a configured number of cycles then the corresponding output signal is set to 1. The same procedure applies for a transition from 1 to 0, with a different configured number of cycles.

The LogicAggregatorGAM in Fig.9b takes a set of logical input signals and a set of enable signals, in equal numbers, and generates an output signal that packs each logical input in a bit after ANDing it with the corresponding enable signal. As an example if there are 32 logical input signals and 32 enable signals each pair is ANDed and all are packed on a 32-bit word that is written to the output signal.

The modules described are used to implement the WALLS checks illustrated in Fig. 10. The initial steps are aimed at establishing conditions to enable the checks. These conditions relate with setting a time window, to make sure the checks are performed only when all systems should be transmitting, or setting plasma conditions, such as a minimum plasma current, power exhaust or given plasma configuration. All checks have also individual global enable signals to prevent a particular check to raise an alarm, a feature that can be used to disable alarms not yet commissioned. After the physical quantities' checks the alarms are condensed, by ORing together the enabled checks of the same type, then hysteresis is applied to avoid spurious trips and finally the alarms aggregated in a single 32-bit word to prepare for transmission via the RTDN.

The result of the checks and alarms are recorded and can be parsed for post-pulse analysis. Each check/alarm is 0 when not asserted and 1 otherwise, thus a single bit is necessary to store it. The set of all checks is stored in a vector of 512 bits and the same goes for the alarms. To store a vector of this magnitude 16 signals of 32-bits each are needed. Not all bits are currently in use, allowing to add more checks/alarms in the future.

The global alarms sent to RTPS are also stored in JPF, but for these a single 32-bit signal suffices. The definition is shown in Table 6 and each bit represents a set of ORed alarm bits. The decision for this particular grouping pertains to the type of stops that can be associated with them. One of those is the Main Chamber Hot Spot stop that is related with an event happening in the main chamber, such as the inner or outer wall overheating. By treating the upper dump plate, inner and outer walls separately it is possible to refine the stop strategy in the future. The same idea applies to the Divertor Hot Spot stop and the corresponding global alarm bits.

4. OPERATIONAL RESULTS

4.1. PERFORMANCE

Figure 11 shows the execution time measurements for each module. These values were obtained during a plasma pulse and thus are taken with the actual configuration file and under operational conditions. The pulse in question is the Pulse number 83794, the last pulse of the C30c experimental campaign. The Felix GAM is the one that takes longer to execute and its behaviour is different with or without plasma, hence the variation between minimum and maximum measured execution times. The limiter power density and thermal calculations follow, mainly due to the number of tiles that need these calculations. The number of checks to perform is also high, explaining the execution time as high as the limiter calculations. Because the total execution time is still under 1ms there was no need to execute these modules in parallel using the WorkLibrary.

The real-time thread total cycle time was also measured to ensure the timing datagram is provided at the correct rate and the jitter caused by it is not exceedingly high. Figure 12 shows the histogram plot of this measurement and the cycle time is close to the expected value at 9.999ms ± 4.382μs. Comparing this jitter with the vertical stabilisation jitter, which is less than 1μs running under RTAI [18], it is high but given the overall cycle time of 9.999ms it represents 0.04%, which can safely be neglected.

4.2. ALARMS

During the C28-C30 experimental campaigns WALLS routinely monitored the ILW. Figure 13 shows an event where a divertor probe measuring the current in the D1 circuit failed. As a consequence the JET shape controller was increasing the voltage in order to drive the requested current, which always measured 0A. The wrong current measurement affected the boundary reconstruction and WALLS detected this as an inner strike-point radial position measurement exceeding the URSI limit. Figure 13 shows, for Pulse number 82957, the URSI strikepoint position. From 6.5s the

inner strike-point started moving inwards, the radial position value started lowering, and close to 8.6s it started to move erratically and remained for over 50ms on the upper region of the divertor (< 2.05m and below the URSI limit). The alarm was raised and successfully transmitted to RTPS, which stopped the pulse.

4.3. LIMITER SURFACE TEMPERATURE

Figure 14 shows the surface temperature calculated by WALLS in real-time during JET pulse number 83620. The corresponding surface temperature measured by the KL7 IR camera is also plotted for comparison. There is a reasonable agreement between calculation and measurement, but a proper and complete evaluation of the models is presently being performed. In this pulse the highest temperature of around 1000^{o}C was measured at tile 6 was properly calculated by WALLS. However it is now known that the real temperature was higher as this tile melted during this pulse. This indicates that the limit needs to be chosen lower than the melting point to cater for this situation.

5. FINAL REMARKS

This paper presents the design, implementation and the first operational results of WALLS for the JET's ILW.

Moving from the VME/PowerPC to the PC/x86 architecture brought the increase in performance required for monitoring the ILW. At present the execution time of all computational modules is under 1ms which leaves sufficient margin for upgrades. WALLS is also the first system enabled to make use of the WorkLibrary, a library developed to take advantage of multi-core processors for real-time parallel work. It means that if more complex models are developed then enough computational capabilities are available. This is an important concept as the future of CPUs involves an increase in the number of computational cores.

Running the code under the Linux OS with real-time features allows a faster development cycle and at the same time a final release with good real-time performance. The modularity of MARTe provides the flexibility to add new features with minimum effort and testing new concepts offline is eased by running the code under Linux OS. Moreover, MARTe is an open-source framework and this is an advantage as it gets support and active development from the community. Also being multi-platform has proven to be beneficial during the hardware evaluation process as it was possible and straightforward to run the same code in different hardware platforms for comparison.

WALLS is a work in progress as the operational experience increases. If WALLS is to be used as a temperature provider when the protection cameras are blinded by the fusion neutrons then the models need to be accurate. Their evaluation is underway by comparing the temperatures with those measured by IR cameras.

Future work also involves tuning and evaluating the H-mode detector, adding a thermal model for the upper dump plate and evaluating the need to add a 2-D thermal diffusion model for the divertor tiles.

ACKNOWLEDGEMENTS

This work, supported by the European Communities under the contract of Association between EURATOM, IST and CCFE, was carried out within the framework of the European Fusion herein do not necessarily reflect those of the European Commission.

REFERENCES

[1]. G. Matthews, M. Beurskens, S. Brezinsek, M. Groth, E. Jorin, A. Loving, M. Kear, M.-L. Mayoral, R. Neu, P. Prior, V. Riccardo, F. Rimini, M. Rubel, G. Sips, E. Villedieu, P. de Vries, M. Watkins, E.- J. Contributors, JET ITER-like wall - overview and experimental programme, Physica Scripta 2011 (2011) 014001. doi:10.1088/0031- 8949/2011/T145/014001.

[2]. V. Riccardo, Engineering challenges of the JET ITER-like Wall, Journal of Nuclear Materials 390-391 (2009) 895–899. doi:10.1016/j.jnucmat.2009.01.230.

[3]. G. Arnoux, S. Devaux, D. Alves, I. Balboa, C. Balorin, N. Balshaw, M. Beldishevski, P.J. Carvalho, M. Clever, S. Cramp, J.-L. de Pablos, E. de la Cal, D. Falie, P. Garcia-Sanchez, R. Felton, V. Gervaise, A. Goodyear, A. Horton, S. Jachmich, A. Huber, M. Jouve, D. Kinna, U. Kruezi, A. Manzanares, V. Martin, P. McCullen, V. Moncada, K. Obrejan, K. Patel, P.J. Lomas, A. Neto, F. Rimini, C. Ruset, B. Schweer, G. Sergienko, B. Sieglin, A. Soleto, M. Stamp, A. Stephen, P.D. Thomas, D.F. Valcárcel, J. Williams, J. Wilson, K.-D. Zastrow, A protection system for the JET ITER-like wall based on imaging diagnostics, Review of Scientific Instruments **83** (10) (2012) 10D727–10D727–3. doi:10.1063/1.4738742.

[4]. Y. Tanimura, T. Iida, Eects of DD and DT neutron irradiation on some Si devices for fusion diagnostics, Journal of Nuclear Materials **258-263** (2) (1998) 1812–1816. doi:10.1016/S0022-3115(98)00142-1.

[5]. A. Cenedese, F. Sartori, V. Riccardo, P. J. Lomas, JET first wall and divertor protection system 68 (2003) 785–790. doi:10.1016/S0920- 3796(03)00317-X.

[6]. F. Piccolo, F. Sartori, L. Zabeo, E. Gauthier, F. Trohay, Upgrade of the power deposition and thermal models for the first wall protection of JET with an ITER-like Be combination of wall materials, Fusion Engineering and Design **82** (5-14) (2007) 1094–1101. doi:10.1016/j.fusengdes.2007.02.032.

[7]. O. Barana, A. Murari, E. Jorin, F. Sartori, Real-time calculation of plasma parameters for feedback control in JET, Nuclear Fusion **44** (2) (2004) 335–341. doi:10.1088/0029-5515/44/2/016.

[8]. B. Xiao, D. Humphreys, M. Walker, A. Hyatt, J. Leuer, D. Mueller, B. Penaflor, D. Pigrowski, R. Johnson, A. Welander, Q. Yuan, H. Wang, J. Luo, Z. Luo, C. Liu, L. Liu, K. Zhang, EAST plasma control system, Fusion Engineering and Design **83** (2-3) (2008) 181–187. doi:10.1016/j.fusengdes.2007.12.028.

[9]. G. Manduchi, A. Luchetta, A. Soppelsa, C. Taliercio, The new feedback control system of RFX-mod based on the MARTe real-time framework, in: 18th IEEE-NPSS Real Time

Conference, IEEE, Berkeley, CA, USA, 2012, pp. 1–5. doi:10.1109/RTC.2012.6418378.

[10]. J. How, The JET Pulse Termination Network, Fusion Technology **2** (1980) 1421–1426.

[11]. D. Alves, R. Felton, S. Jachmich, P. Lomas, P. McCullen, A. Neto, D. F. Valcárcel, G. Arnoux, P. Card, S. Devaux, A. Goodyear, D. Kinna, A. Stephen, K.-D. Zastrow, Vessel thermal map real-time system for the JET tokamak, Physical Review Special Topics - Accelerators and Beams **15** (5) (2012) 054701. doi:10.1103/PhysRevSTAB.15.054701.

[12]. A. Stephen, D. Alves, G. Arnoux, T. Budd, P. Card, S. Devaux, R. Felton, A. Goodyear, J. Harling, S. Jachmich, D. Kinna, P. Lomas, P. Mccullen, A. Neto, P. Thomas, D. F. Valcárcel, I. Young, K.-d. Zastrow, Centralised Coordinated Control to Protect the JET ITER-Like Wall, in: Proceedings of the 13th International Conference on Accelerator and Large Experimental Physics Control Systems, no. 11, Grenoble, France, 2011.

[13]. P.C. Stangeby, The Plasma Boundary of Magnetic Fusion Devices, 1st Edition, IOP Publishing Ltd., 2000.

[14]. S. González, J. Vega, A. Murari, A. Pereira, S. Dormido-Canto, J. M. Ramírez, Automatic location of L/H transition times for physical studies with a large statistical basis, Plasma Physics and Controlled Fusion **54** (6 (2012) 065009 (19pp). doi:10.1088/0741-3335/54/6/065009.

[15]. Y. R. Martin, T. Takizuka, t. I. C. H.-m. T. D. Group, Power requirement for accessing the H-mode in ITER, Journal of Physics: Conference Series 123 (1) (2008) 1–11. doi:10.1088/1742-6596/123/1/012033.

[16]. Y. Andrew, N.C. Hawkes, M.G. O'Mullane, R. Sartori, M.D. Baar, I. Coey, K. Guenther, I. Jenkins, A. Korotkov, P. Lomas, G.F. Matthews, A. Matilal, R. Prentice, M. Stamp, J. Strachan, P.D. Vries, J.E. Contributors, JET divertor geometry and plasma shape effects on the L-H transition threshold, Plasma Physics and Controlled Fusion **46** (5A) (2004) A87–A93. doi:10.1088/0741-3335/46/5A/009.

[17]. R. Felton, K. Blackler, S. Dorling, A. Goodyear, O. Hemming, P. Knight, M. Lennholm, F. Milani, F. Sartori, I. Young, Real-time plasma control at JET using an ATM network, in: 11th IEEE NPSS Real Time Conference, IEEE, Santa Fe, 1999, pp. 175–181. doi:10.1109/RTCON.1999.842597.

[18]. A. Neto, F. Sartori, F. Piccolo, R. Vitelli, G. D. Tommasi, L. Zabeo, A. Barbalace, H. Fernandes, D. F. Valcárcel, A. J. N. Batista, J.-e. Contributors, MARTe : A Multiplatform Real-Time Framework, IEEE Transactions on Nuclear Science **57** (2) (2010) 479–486. doi:10.1109/TNS.2009.2037815.

[19]. P. J. Carvalho, P. Duarte, T. Pereira, R. Coelho, C. Silva, H. Fernandes, Real-Time Tomography System at ISTTOK, IEEE Transactions on Nuclear Science **58** (4) (2011) 1427–1432. doi:10.1109/TNS.2011.2152853.

[20]. L. Boncagni, Y. Sadeghi, D. Carnevale, G. Mazzitelli, A. Neto, D. Pucci, F. Sartori, F. Piesco, S. Sinibaldi, V. Vitale, R. Vitelli, L. Zaccarian, S. Monaco, G. Zamborlini, First Steps in the FTU Migration Towards a Modular and Distributed Real-Time Control Architecture Based

on MARTe, IEEE Transactions on Nuclear Science **58** (4) (2011) 1778– 1783. doi:10.1109/TNS.2011.2158851.

[21]. D. Alves, A. Neto, D.F. Valcárcel, R. Felton, J. Lopez, A. Barbalace, L. Boncagni, P. Card, G. De Tommasi, A. Goodyear, S. Jachmich, P. Lomas, F. Maviglia, P. McCullen, A. Murari, M. Rainford, C. Reux, F. Rimini, F. Sartori, A. Stephen, J. Vega, R. Vitelli, L. Zabeo, K.-D. Zastrow, J. E. Contributors, A New Generation of Real-Time Systems in the JET Tokamak, in: 18th IEEE-NPSS Real Time Conference, Berkeley, CA, USA, 2012. doi:10.1109/RTC.2012.6418367.

[22]. A. Neto, D. Alves, L. Boncagni, P.J. Carvalho, D.F. Valcárcel, A. Barbalace, G. De Tommasi, H. Fernandes, F. Sartori, E. Vitale, R. Vitelli, L. Zabeo, A Survey of Recent MARTe Based Systems, IEEE Transactions on Nuclear Science **58** (4) (2011) 1482–1489. doi:10.1109/TNS.2011.2120622.

[23]. O. Barana, E. Jorin, A. Murari, F. Sartori, Real-time determination of confinement parameters in JET, Fusion Engineering and Design **66-68** (2003) 697–701. doi:10.1016/S0920-3796(03)00331-4.

[24]. D.F. Valcárcel, D. Alves, A. Neto, C. Reux, B.B. Carvalho, R. Felton, P. J. Lomas, J. Sousa, L. Zabeo, JET EFDA contributors, Parallel Task Management Library for MARTe, in: 18th IEEE-NPSS Real Time Conference, Berkeley, CA, USA, 2012. doi:10.1109/RTC.2012.6418375.

[25]. D.P. O'Brien and J.J. Ellis and J. Lingertat, Local expansion method for fast plasma boundary identification in JET, Nuclear Fusion **33** (3) (1993) 467–474. doi:10.1088/0029-5515/33/3/I08.

[26]. L. Zabeo, G. Artaserse, A. Cenedese, F. Piccolo, F. Sartori, A new approach to the solution of the vacuum magnetic problem in fusion machines, Fusion Engineering and Design **82** (5-14) (2007) 1081–1088. doi:10.1016/j.fusengdes.2007.04.028.

[27]. F. Sartori, A. Cenedese, F. Milani, JET real-time object-oriented code for plasma boundary reconstruction, Fusion Engineering and Design **68** (2003) 735–739. doi:10.1016/S0920-3796(03)00290-4.

[28]. M. Lennholm, T. Budd, R. Felton, M. Gadeberg, A. Goodyear, F. Milani, F. Sartori, Plasma control at JET, Fusion Engineering and Design **48** (1-2) (2000) 37–45. doi:10.1016/S0920-3796(00)00125-3.

[29]. I. Nunes, P. de Vries, P. Lomas, Optimization of the JET beryllium tile profile for power handling, Fusion Engineering and Design **82** (15-24) (2007) 1846–1853. doi:10.1016/j.fusengdes.2007.04.047.

System	CPU				Memory	PTN Connection	OS
	Model	Cores	Frequency	L2 Cache			
MVME 5100	PowerPC MPC7410	1	400 MHz	Up to 2 MB (no L3)	32 MB	Yes	VxWorks
MVME 5500	PowerPC MPC7455	1	1.0 GHz	256 kB	512 MB	Yes	VxWorks
PC Intel	Q6600	4	2.4 GHz	4 MB	2 GB	No	Linux
PC AMD	Athlon II X4 640	4	3.0 GHz	4×512 kB	2 GB	No	Linux

Table 1: Systems considered and evaluated for the WALLS processing hardware.

System	Execution time (μs)	Execution jitter (%)	Cycle time (ms)	Cycle time jitter (%)
MVME 5100	111.6 ± 3.57	3.2	10.0001 ± 0.0022	0.022
MVME 5100	66.6 ± 0.88	1.3	9.9999 ± 0.0033	0.033
PC Intel	4.8 ± 0.86	17.7	10.0000 ± 0.0157	0.16
PC AMD	3.3 ± 0.09	2.8	10.0000 ± 0.00048	0.0048

Table 2: Statistical measurement of the execution and cycle times for each system.

Parameter	Value
CPU	Model: AMD Phenom II Core count: 6 Clock frequency: 3.2 GHz Cache L1 (Instructions + Data): 6×64 + 6×64 kB Cache L2: 6×512 kB Cache L3: 6 MB (shared)
Memory	8 GB Integrated DDR2/DDR3 Memory Controller
Motherboard	ASRock 890GX Extreme 4
Disabled BIOS options	Turbo Core Technology Cool'n'Quiet Enhanced Halt State CPU Thermal Throttle
Operating system	Linux Fedora Core 12
Kernel boot option	isolcpus=1,2,3,4,5; idle= mwait

Table 3: Final hardware and software solution adopted for the WALLS system.

Plasma configuration	Value
Undetermined	–1
Limited	0
Lower diverted	1
Upper diverted	2

Table 4: Plasma configuration and the value that is written as an output signal on the DDB.

Plasma configuration	Condition	Value
Undetermined		–1
L-mode	$\frac{P_{exh}}{P_{L-H}} < \eta$	0
H-mode	$\frac{P_{exh}}{P_{L-H}} \geq \eta$	1

Table 5: Plasma mode and the value that is written as an output signal on the DDB.

Bit	Alarm
0	Blind
1	Lower strike-points and X-point
2	Reserved for upper strike-points and X-point
3	Gaps
4	Divertor temperature and energy
5	reserved for upper dump plate temperature
6	Inner limiter temperature
7	Outer limiter temperature
8-31	Not used

Table 6: Definition of the global alarm sent to RTPS.

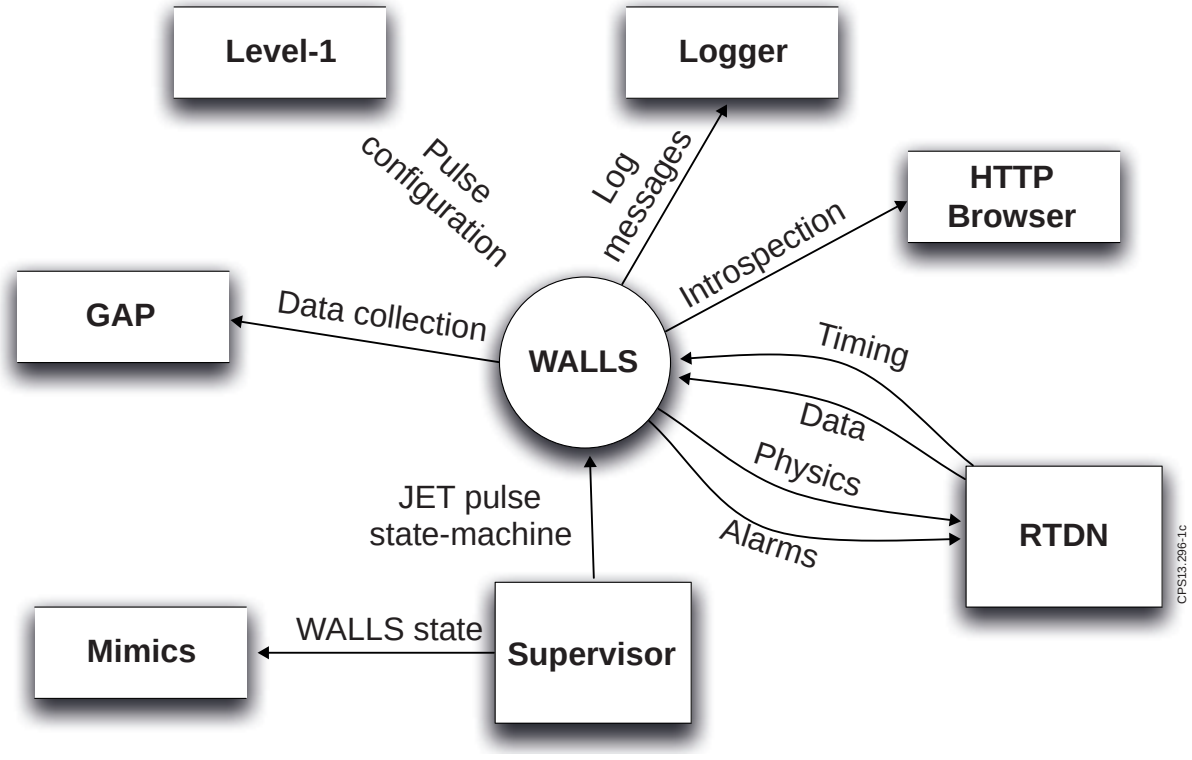

Figure 1: The JET CODAS context diagram showing the systems WALLS interacts with.

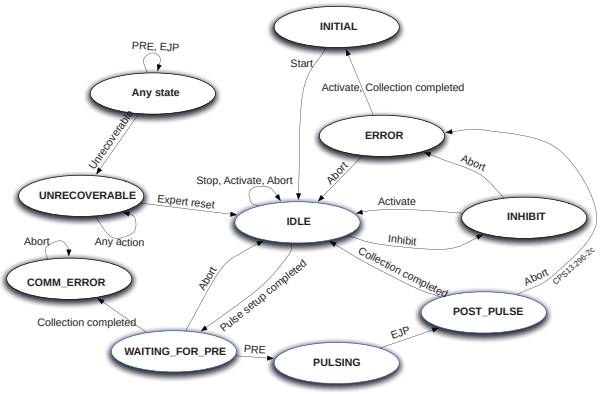

Figure 2: Diagram of the WALLS state-machine driven by the supervisory system. The main states, through which the system is taken during a normal pulse, are represented in blue.

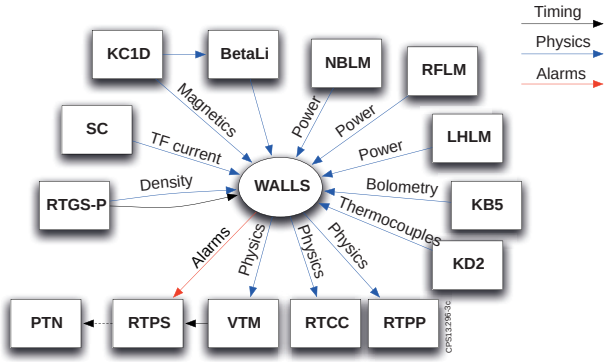

Figure 3: RTDN context diagram showing the interaction between systems in the RTDN.

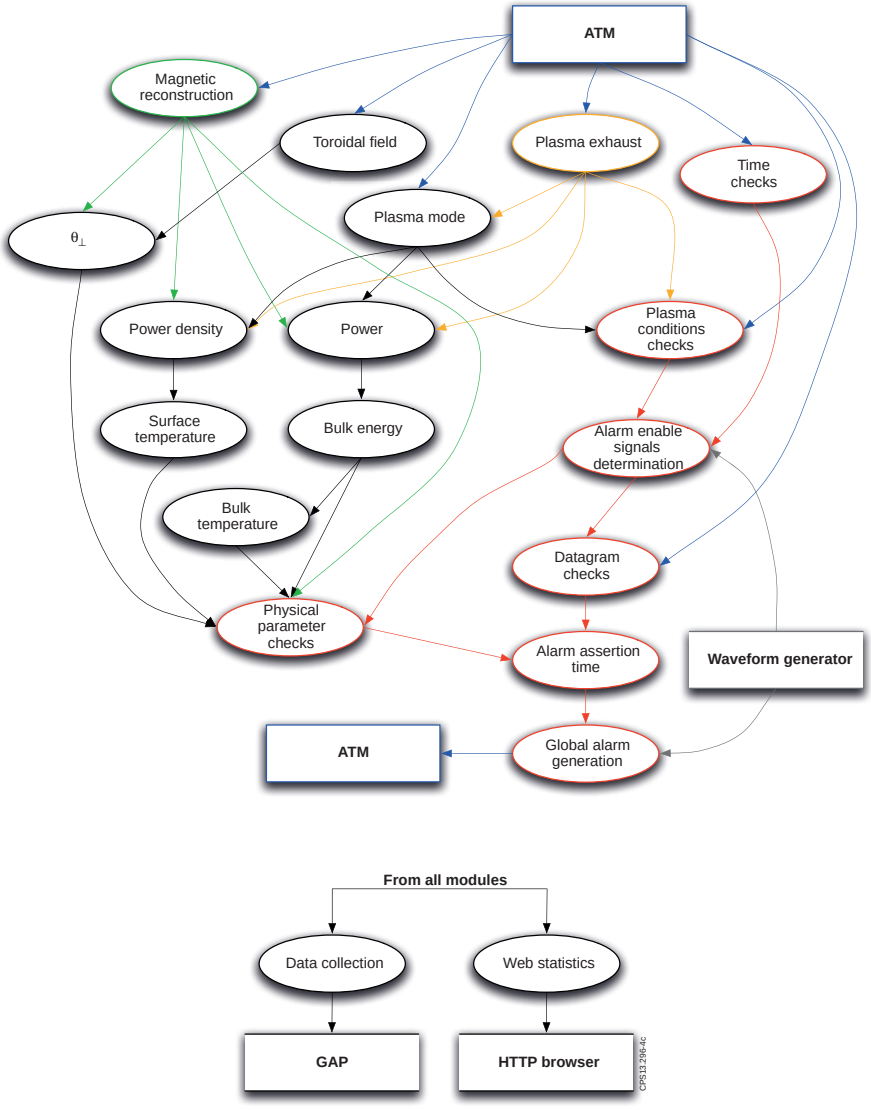

Figure 4: Data flow diagram illustrating the functional behaviour of WALLS.

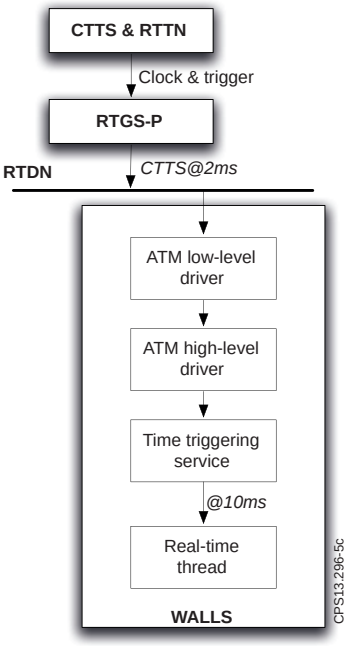

Figure 5: Timings diagram showing the flow of the timing information from the CTTS source to the real-time thread in WALLS.

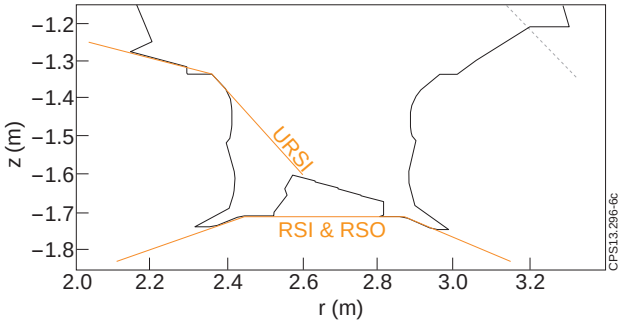

Figure 6: The WALLS URSI strike-point definition on the divertor.

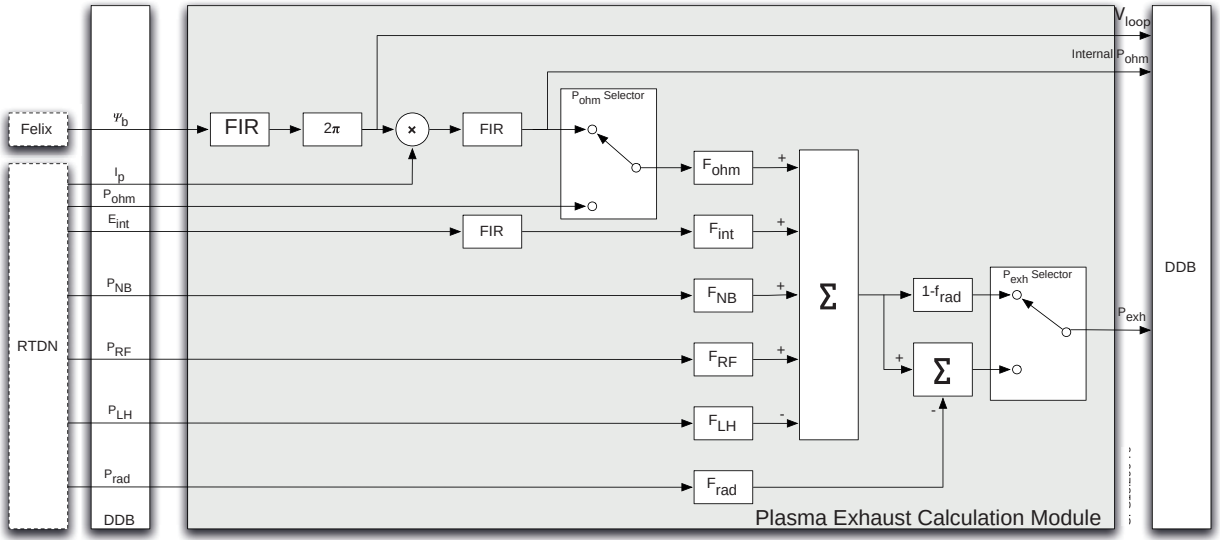

Figure 7: Plasma exhaust calculation module internal diagram.

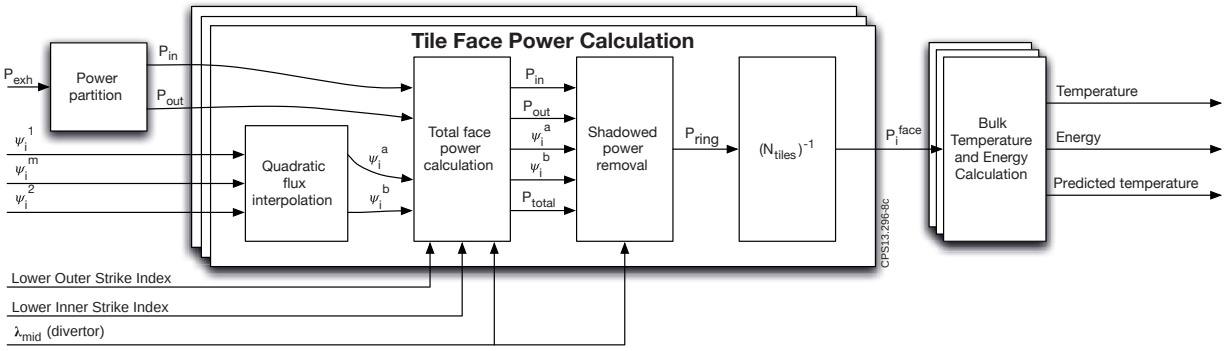

Figure 8: The divertor thermal calculations modules. The calculation of the power on each face i is performed taking into account the position of the strike-points and the shadowing effect on the divertor.

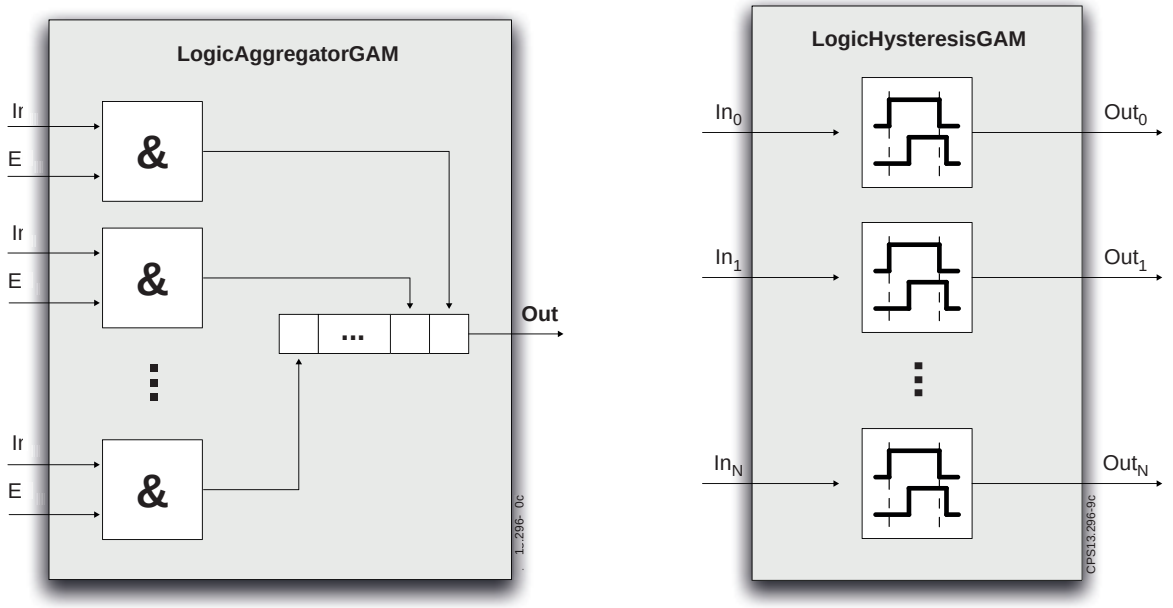

Figure 9: Hysteresis and aggregation of logical signals.

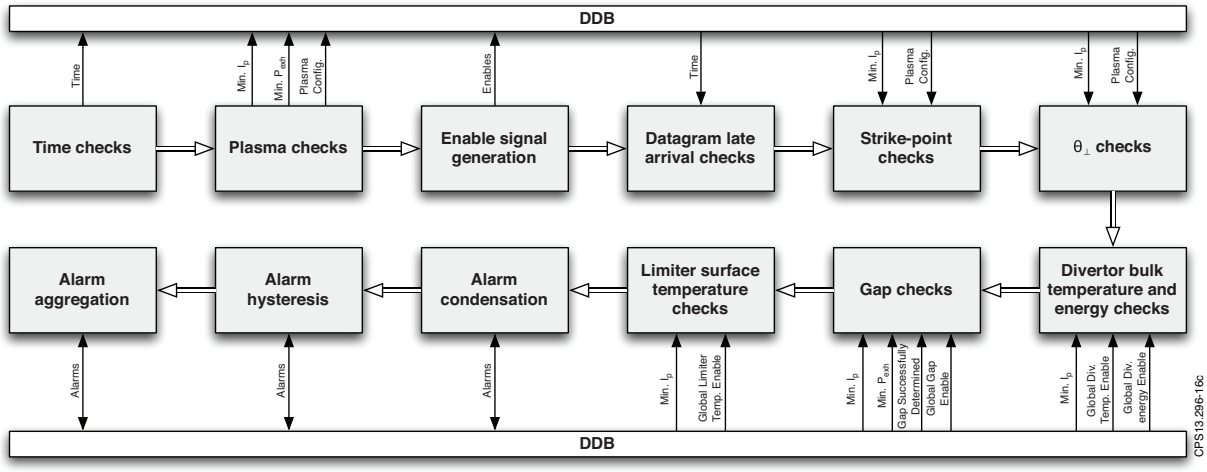

Figure 10: Diagram that illustrates the steps and the order on which the checks are performed.

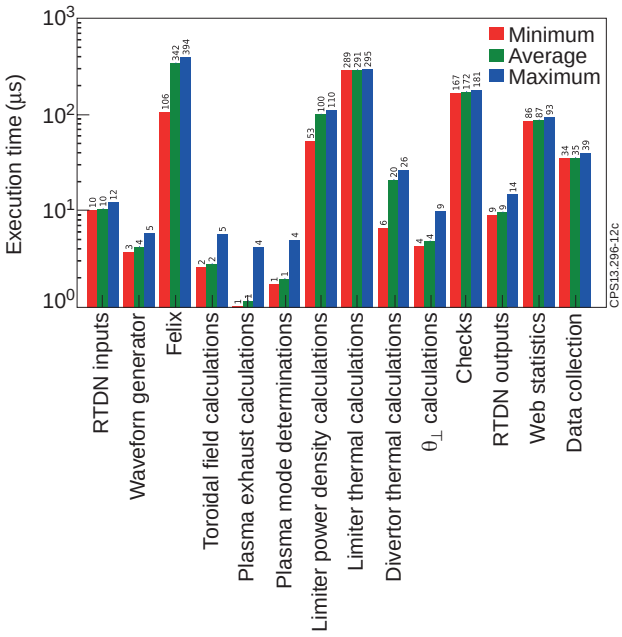

Figure 11: Execution time for the WALLS' modules for JET Pulse No: 83794. The discrepancy between minimum, maximum and average times measured on some of them stems from the fact that they may have dierent behaviour with or without plasma.

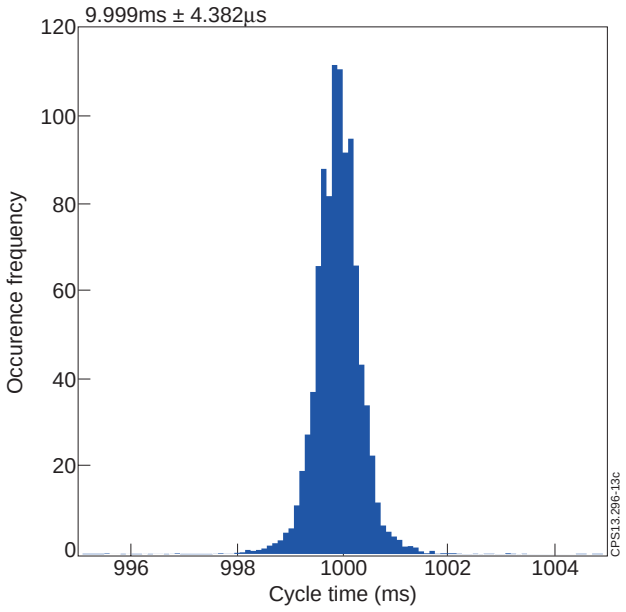

Figure 12: Cycle time measurement for JET Pulse No: 83794. The cycle time is close to the expected 10ms and the jitter is substantially low and of the order of a few µs.

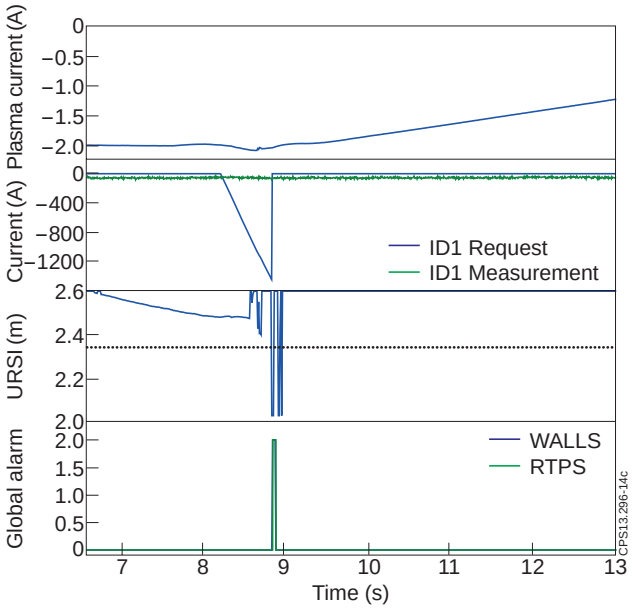

Figure 13: URSI trip on JET Pulse No: 82957. The dashed line shows the URSI limit and, at 8.6s, when the signal is below the limit for more than 50ms the alarm is raised. The D1 current request was increasing whereas the measurement was zero throughout the pulse. This led to a wrong plasma configuration with the subsequent URSI trip.

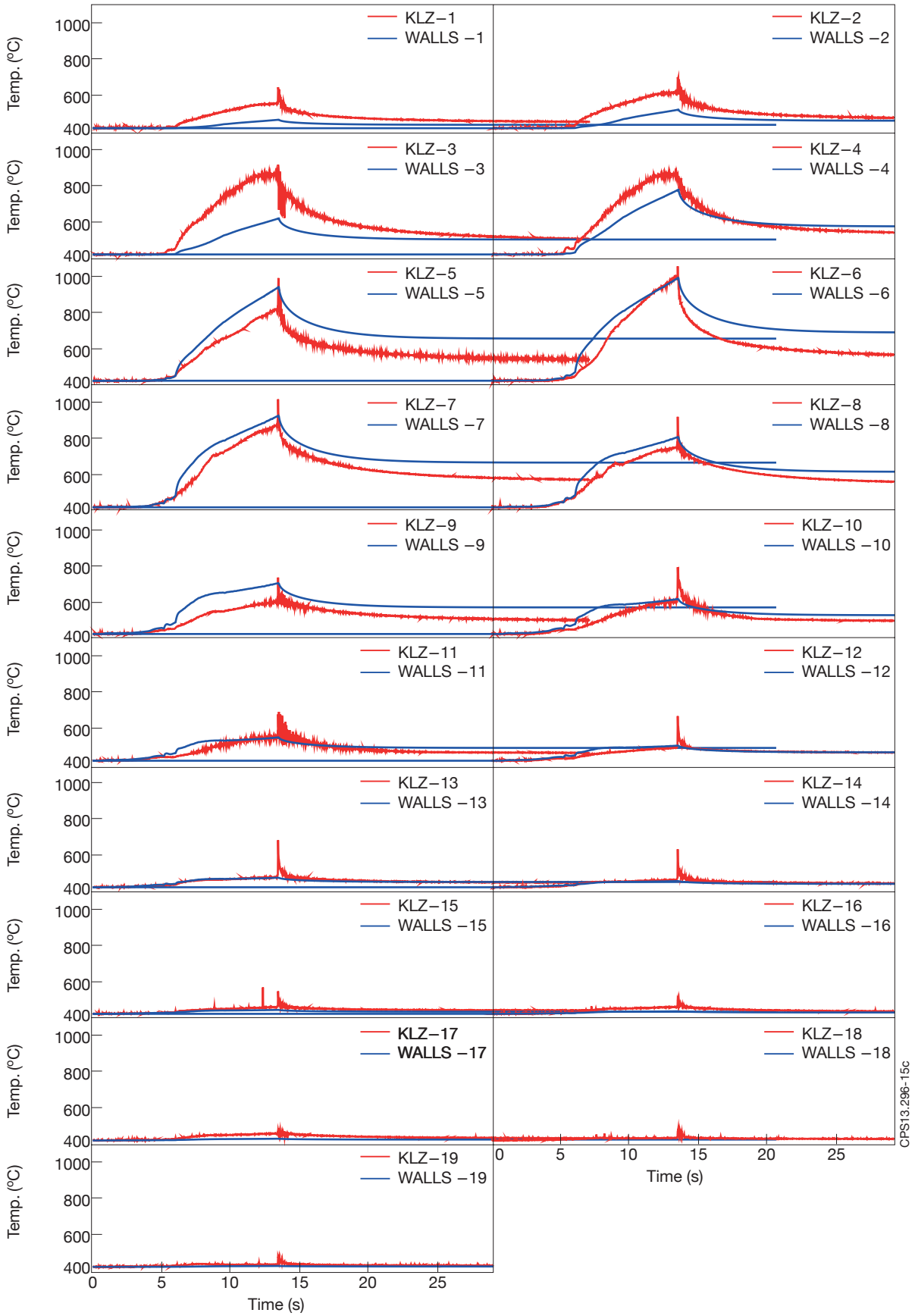

Figure 14: IWGL tiles' surface temperature calculated in realtime by WALLS for λ = 1cm and the corresponding measurement by the KL7 IR camera for comparison for the limited JET Pulse No: 83620. The contact point was on tile 6.