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Real-Time Algorithms for JET Hard X-Ray and Gamma-Ray Profile Monitor

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A. Fernandes[1], R.C. Pereira[1], D.F. Valcárcel[1], D. Alves[1], B.B. Carvalho[1],
J. Sousa[1], V. Kiptily[2], C.M.B.A. Correia[3], B. Gonçalves[1]
and JET EFDA contributors*

JET-EFDA, Culham Science Centre, OX14 3DB, Abingdon, UK

[1]*Associação EURATOM/IST, Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico,
Universidade Técnica de Lisboa, 1049-001 Lisboa, Portugal*
[2]*EURATOM-CCFE Fusion Association, Culham Science Centre, OX14 3DB, Abingdon, OXON, UK*
[3]*Centro de Instrumentação, Dept. de Física, Universidade de Coimbra, 3004-516 Coimbra, Portugal*
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ABSTRACT

The steady state operation with high energy content foreseen for future generation of fusion devices will necessarily demand dedicated real-time tools and mechanisms for data handling and machine control. Consequently, the real-time systems for those devices should be carefully selected and their capabilities previously established. The Joint European Torus (JET) is undertaking an enhancement program, which includes tests of relevant real-time tools for the International Thermonuclear Experimental Reactor (ITER), a key experiment for future fusion devices. In these enhancements is included a new Data AcQuisition (DAQ) system, with real-time processing capabilities, for the JET hard X-ray and gamma-ray profile monitor. The DAQ system is composed by dedicated digitizer modules with embedded Field Programmable Gate Array (FPGA) devices. The interface between the DAQ system, the JET Control and Data Acquisition System (CODAS) and the JET Real-Time Data Network (RTDN) is provided by the Multithreaded Application Real- Time executor (MARTe). This paper describes the real-time algorithms, developed for both digitizers' FPGAs and MARTe application, capable of meeting the DAQ real-time requirements. The new DAQ system, including the embedded real-time features, was commissioned during the 2012 experiments. Results achieved with these real-time algorithms during experiments are presented.

1. INTRODUCTION

The recent availability of ultra-high frequency (GByte=s) Data AcQuisition modules (DAQ) necessarily increase the needs of dedicated real-time data processing algorithms for a wide range of applications [1]. These modules are able to produce large amounts of data thus leading to storage problems. Real-time tools and algorithms are also required by the expected steady state operation of next fusion devices for sustainable energy production. In continuous operation, data must be processed in real-time, storing only selected information, and simultaneously guaranteeing an effective plasma control [2]. The Joint European Torus (JET) is undertaking an enhancement program where real-time tools and mechanisms for data-handling and machine control are being tested. These enhancements include a new DAQ system, based on Advanced Telecommunication Computer Architecture (ATCA®), for digitizing the hard X-ray and gamma-ray signals detected by the 19 Fast Electron Bremsstrahlung (FEB) detectors (CsI(Tl) scintillators coupled to photodiodes), installed at JET profile monitor [3]. This ATCA-based DAQ system, developed at Instituto de Plasmas e Fus~ao Nuclear (IPFN), was expected to overcome the former FEB diagnostic limitations and simultaneously exploit required real-time features [4]. ATCA has been extensively used for control and data acquisition systems for fusion experiments [5]. Moreover, ATCA-based control and data acquisition are also being considered for the International Thermonuclear Experimental Reactor (ITER) Fast Plant System Controller (FPSC), an extensive prototyping program whose specification will be applicable to several diagnostic systems targeting plasma control [6].

The ATCA-based DAQ system installed at JET is composed by a commercial ATCA shelf, an ATCA controller [7] with an Intel® Core™ 2 Duo ×86 processor, three fast digitizer modules [8] to cover all the 19 channels, and a commercial Peripheral Component Interconnect (PCI)/

Asynchronous Transfer Mode (ATM) module. Each digitizer module is composed by eight 13-bit resolution Analog to Digital Converters (ADCs) with a sampling rate up to 250MSPS, 4GB DDR2 SODIMM local memory, and two Field Programmable Gate Array (FPGA) devices from Xilinx (XC4VFX60/1152). Besides the basic module functionalities, FPGAs are used for realtime data reduction and pulse processing, being capable of delivering in real-time the energy of the pulses acquired from the 19 FEB detectors. The PCI/ATM module is mandatory for connecting to the JET Real-Time Data Network (RTDN), an ATM network for the real-time interchange of data between diagnostics and control systems, foreseeing control purposes [4]. The interface to the JET Control and Data Acquisition System (CODAS) and to the JET RTDN is provided by the Multithreaded Application Real-Time executor (MARTe) [9], a C++ framework used in several fusion machines and installed at the ATCA controller. The MARTe-based application is running under the Linux R OS with the kernel version 2.6.35.9. To cope with the DAQ real-time requirements, and foreseeing new real-time applications, several real-time algorithms were developed, implemented and tested in the DAQ system. They can be divided in: (i) algorithms for digitizers' FPGAs and (ii) algorithms for MARTe application. The developed algorithms are described in sections 2 and 3, highlighting that some of them are not currently being used by the new hard X-ray and gammaray profile monitor diagnostic. The achieved results are presented in section 4, followed by the conclusions.

2. REAL-TIME ALGORITHMS FOR FPGA

FPGAs have become increasingly used for real time algorithm processing and data transfer in instrumentation modules, due to its: (i) inherent parallelism of logic resources; (ii) flexibility in its configuration and (iii) unique performance at high frequencies [10]. With a suitable processing algorithm running in the FPGA it is possible to extract in real-time only the key information, leading to a significant data reduction. The FPGA algorithms are easily upgraded (e.g. due to signal changes after replacing detectors), ensuring a correct real-time analysis. Moreover, the FPGA is capable of processing different algorithms simultaneously which can be advantageous for some applications [11].

Different real-time processing algorithms, developed for the digitizer modules' FPGAs, were used for testing the DAQ system, firstly in laboratory, then in-situ with radioactive sources, and finally with plasma during JET experiments. Furthermore, the different algorithms were required to accomplish with two distinct hardware setups (with and without a shaping amplifier in the signal path), deployed during the phase tests. These FPGA algorithms are presented in the following subsections. For their validation, the real-time processed data from the FPGA was compared with data from post-processing algorithms developed in MATLAB. The post-processing algorithms were applied to raw data acquired in the same working conditions.

2.1. ALGORITHM FOR GAUSSIAN SHAPED PULSES

A real-time algorithm was developed and implemented at the digitizer modules' FPGAs in order to calculate the amplitude of Gaussian shaped pulses, obtained when an external shaping amplifier is placed between the detectors and the digitizers. Considering that the pulses amplitude is

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proportional to the energy of the corresponding photon that interacts in the detector, every time a threshold is reached the algorithm starts to find the maximum amplitude, as depicted schematically in figure 1. If no other maximum occurs during the expected pulse duration, defined by the settled shaping time, the achieved maximum value is stored with the corresponding time-stamp, in a 64–bit word.

A shaping amplifier is commonly used for improving the Signal to Noise Ratio (SNR), for baseline restoring, and for rejecting pile-up [12]. However, its presence in the signal path changes the signal source before being digitized, and rejects important information that can be treated digitally (e.g.pile-up). Consequently, the direct connection is a preferable setup, mainly when fast digitizer modules are used. However, it became evident while testing that, due to the poor SNR of the FEB detectors, it was of crucial importance having external shaping amplifiers in the signal path, the same setup used by the former DAQ system [11]. This setup allowed to emphasize the incoming pulses, and the algorithm applied to Gaussian shaped pulses was used to attest that the pulses could be detected. The algorithm was important to conclude that the maximum ADC sampling rate (250MHz) was too high for sampling the incoming signals. The effective number of bits increases if the signal is down-sampled and, consequently, the pulses with less resolution become more visible [11].

2.2. ALGORITHM FOR RAMP-LIKE PULSES

If the signals from the detectors are directly connected to the digitizer modules' ADCs, all data processing functions, such as filtering and shaping, baseline restoration, ballistic deficit correction, and pileup reject/resolving, need to be executed digitally [13]. A common pulse shape returned by gamma-ray/X-ray spectroscopy detectors is similar to an exponential signal with a fast positive or negative step (rise time) followed by a long decay step (decay time) [12]. The amplitude of the fast step is proportional to the energy deposited by gamma-ray (high energy pulses) or X-ray (lower energy pulses) in the detector [12]. The trapezoidal shaper is a quasi-optimum filter widely used in spectroscopy analyses [14], being capable to suppress ballistic deficit responsible for reducing the spectrometers resolution, observed in the presence of pulses with sharp peaks (e.g. gamma-ray, X-ray pulses). When the trapezoidal shaper is applied the exponential signal is transformed into a trapezoid, where the difference between the flat top and the base corresponds to the pulse energy [14].

The conventional Digital Trapezoidal Shaper (DTS) [14] is composed by: two delay-subtract units where data is delayed by k and l values, respectively, and subtracted to the present data; one High Pass Deconvolver (HPD); and a final accumulator (ACC) [14]. The processing algorithm implemented in the DAQ's FPGAs is based on the conventional DTS however with some adjustments. Besides the poor SNR, the CsI(Tl) photodiode detectors present pulses with very long decay (rise time of 200ns and pulse duration > 400μs), similar to ramp-like pulses instead of exponentials. Accordingly, if the conventional DTS is applied to the incoming pulses, the corresponding trapezoids remain superimposed, making it impossible to distinguish pulse signals from noise. Considering that the HPD stage is used to deconvolve the high-pass filters response, meaning that when applied to

exponential signals they are converted into step signals [14], if the acquired pulses are assumed as the step signal itself the HPD stage can be avoided. When this adapted filter was applied to the incoming ramp-like signals, the filtered pulses were similar to Gaussians instead of trapezoids, as depicted in figure 2 diagram. This Digital Ramp to Gaussian Shaper (DRGS) allowed to reduce the shaping time considerably, avoiding superimposed pulses.

Due to the poor SNR ratio presented by CsI(Tl) signals, associated with long decay time pulses, the best results were achieved when the DRGS stage was applied twice. Therefore, the implemented real-time algorithm for processing directly the hard X-ray and gamma-ray pulses from FEB detectors is composed by a Double-DRGS followed by a final ACC stage (D-DRGS), as depicted in figure 3. The signal changes across the filter depicted in a) highlight the importance of applying two DRGS stages for low energy pulses. As shown, the pulse is still embedded in noise after the first DRGS. From signal b) evolution is evidenced the algorithm capability in resolving superimposed pulses. Simultaneously with the D-DRGS unit, an Edge-Detector (ED) stage (figure 3) triggers every time data reaches a predefined threshold. The threshold settles the limit between noise/baseline of the filtered signal, and its value is detector's dependent. As so, each channel has a different value that must be properly calculated. For this purpose the FPGA code includes an off-line calibration operation mode for computing threshold values. Finally, when a trigger event is signaled the Energy Resolver (ER) stage starts to calculate the corresponding pulse energy. It was stipulated that if no other trigger events occur during 2k+l inputs (number of samples required for a well defined filtered pulse), the energy of this event corresponds to the maximum amplitude during that interval. The achieved energy value is stored with the corresponding time-stamp in a 64–bit word.

The two's complement arithmetic, a collection of mathematical rules for computing signed binary numbers [15], was the solution adopted to efficiently make at FPGA the D-DRGS operations. Furthermore, before each ACC stage, data is truncated in the Least Significant Bits (LSB) part and the same number of Most Significant Bits (MSB) are created, guaranteeing the same 32–bit number. Once more, this ensures that sums and multiplications do not overflow. Finally the D-DRGS output is truncated to the 16 most significant bits, converting it to a 16–bit word, as required by the next FPGA stage.

2.3. PARALLELIZED DTS FOR HIGH SPEED APPLICATIONS

Foreseeing improvements on cabling and a new set of detectors, the DAQ system can take advantage of its maximum ADC's sampling rate (250MSPS). Moreover, if even higher sampling rates are required, one option can be to replace the digitizer modules' ADCs by the compatible 400MSPS solution [16]. Another possibility is interleaving channels (e.g. 500MSPS can be achieved by interleaving two channels). The last solution consequently requires extra digitizer modules to cover the 19 detectors. At such high sampling rates (400MSPS), FPGA's are the only fast programmable devices that can be used for both data transfer and processing. However some FPGA resources may present speed limitations (e.g., the 400MSPS exceeds the Virtex-4 FIFO range [17]), leading

to an unavoidable data loss. One possible solution is the input signal parallelization, for reducing its sampling rate inside FPGA without data losses. A parallel pulse processing algorithm, based on the conventional DTS was developed and tested in the digitizer modules, and is expected to be used in a future diagnostic upgrade. Moreover, it was already implemented in another diagnostic at JET, which uses a similar DAQ system although with the 400MSPS ADCs compatible solution [18]. The novelty presented by this algorithm is the capability to perform pulse processing regarding parallel data as if it was in series, meeting the trapezoidal shaper requirements whose output always depends on previous inputs. To do that the acquired data was parallelized and resampled to one fourth of the original rate immediately after being digitized. The developed parallel algorithm is composed by the parallelized DTS unit, the parallelized ED stage and the parallelized ER stage. The parallelized DTS unit is similar to the conventional DTS, considering however four samples in parallel for the recursive algorithm [18]. The ED stage triggers each time one of the four parallel data streams reach the predefined threshold, returning a 4–bit word with the corresponding bit high [18]. Finally, when one of the four ED trigger occurs, the ER stage starts to calculate the pulse energy by the difference between the trapezoid's flat top and baseline, from the parallelized filtered signal [18]. Just like the previous algorithms, if no other trigger occurs during that event, the ER stage returns a 64–bit word with the energy value plus the corresponding time-stamp.

2.4. EVENTS SELECTION ALGORITHM

The algorithms described in sections 2.1, 2.2 and 2.3 provide just the energy values with the corresponding time-stamp of acquired pulses. If it is required to store the pulses itself, and not only its energy values, a different algorithm should be used. An event selection algorithm is requested when it is unfeasible to store all data in the digitizers memory and if the available real-time processing algorithms are not suitable for the acquired pulses. Furthermore, the event selection algorithm is advantageous when it is necessary to store bursts of data for post-processing (e.g. for validation purposes). To meet this requirements an event selection algorithm was developed for the digitizer modules' FPGAs, as depicted in figure 4 flowchart. A circular buffer is used to temporarily store data delayed according with the Pre-TRiGger (PTRG) value settled by the user. The data burst (e.g. pulse) can be signaled with a predefined threshold or by an external trigger. To store the pulses from the CsI(Tl) detectors, and considering the diagnostic's poor SNR, the ED is applied to the filtered signal described in section 2.2 instead of to the input data. When an event is detected in the filtered signal, the FPGA starts storing the input data corresponding to that event. Consequently the input data is delayed to be properly aligned with the ED(t) signal. Each stored event is composed by a 64–bit time-stamp followed by a predefined number of samples (PWIDTH), including the PTRG samples required to provide the baseline level for that event.

3. SOFTWARE MODULES FOR MARTE FRAMEWORK

One of the diagnostic enhancements is the connection to JET's ATM-based RTDN, for real-time analysis and control purposes. MARTe provides a modular seamingless integration of the PCIATM

card into the application mainly due to its strong philosophy of decoupled real-time processing and I/O. Foreseeing general purpose applications of the diagnostic's real-time data made available to the RTDN, a generic datagram definition has been provided. A total of 8 fixed size vectors able to hold experiment dependent output data easily reconfigurable whithin MARTe. For this purpose, dedicated MARTe modules are required to process the signals subsequently made available to the RTDN.

3.1. REAL-TIME SPECTRUM MODULE

The first real-time application for the ATM connection was the capability to provide a datagram in every 2ms containing the pulse counts in pre-defined energy windows, of the most relevant detectors. For that purpose a generic module called spectrum-module was developed to build calibrated spectra for a single channel, and determine from those spectra the total counts in predefined energy windows.

As depicted in figure 5, the module receives the energy values processed by the FPGA, and streamed during acquisition in every 2ms, builds the histogram, calibrates the histogram in counts/energy by using a pre-defined calibration slope for each channel, and delivers to the ATM network datagram the total counts for each pre-defined energy window. To guarantee the timing requirements, avoiding losing packets, the spectrum-module complies with the 2ms of cycle time imposed by the MARTe-based application, depicted in the histogram from figure 6. The execution time measured for each spectrum-module instance, was 20μs with a maximum jitter of 14μs, as depicted the histogram from figure 7. These values were obtained when all range of energies (0–330000a.u.) were used to produce spectra, distributed by 2048 energy bins. If lower values of energy bins or energy range were used, the execution time would be improved.

4. RESULTS

During system integration at JET several tests were performed, firstly without plasma. To obtain expected calibrated spectra, acquisitions were made in presence of radioactive sources, such as a 22Na source embedded in the detectors set, emitting two gamma-ray peaks at 511keV and 1275keV, and a 137Cs source embedded in collimators, emitting a 662keV peak. To cope with the very low activity of these sources (6 25 counts/s) real-time processed data was advantageous for building spectra in time and with enough statistics. Furthermore, the real-time processing algorithms described in sections 2.1 and 2.2 (algorithm for Gaussian shaped pulses and algorithm for ramp-like pulses) were both used during the phase tests. When the algorithm for Gaussian pulses was used, spectroscopy shaping amplifiers needed to be mounted in the signals path, similarly to the former FEB system. As explained before, the Gaussian algorithm was essential to start acquiring suitable spectra and to conclude that the ADCs should not operate at its maximum sampling rate. In figure 8 is depicted a calibrated spectra obtained at JET with algorithm for Gaussian shaped pulses in presence of ^{22}Na and ^{137}Cs radioactive sources.

After down-sampling the acquisition rate to 2.5Msamples=s, considered the most suitable sampling rate taking into account the noisy incoming signals, calibrated spectra were produced with the algorithm for ramp-like pulses, as depicted in the example from figure 9. A similar post processing

algorithm was used to study the pulses stored with the events selection algorithm (section 2.4) and to find the best parameters for the real-time processing.

From results obtained firstly without plasma and later during JET experiments, it was concluded that the algorithm for ramp-like pulses is the best solution, allowing to measure both hard X-ray and gamma-ray, covering an energy range from ~200keV to ~10MeV. When the Gaussian algorithm is used the energies range is limited by the shaping amplifier gain.

The DAQ system was successfully commissioned during 2012 JET experiments and the results obtained with the real-time processing algorithm for ramp-like pulses were validated in a dedicated session. It was concluded that the results obtained from processed data at FPGA are in agreement with the plasma conditions and with other JET diagnostics. As example, figure 10 shows spikes from runaways observed in both horizontal and vertical channels during ramp-up in Pulse No: 82079. These results are consistent with results observed by other JET diagnostics [19].

The spectrum-module algorithm (section 3.1) is used during the discharge to produce counts in energy windows for the ATM datagram every 2ms. Accordingly, a new datagram is sent through JET real-time network every 2ms foreseeing control purposes. In figure 11 are depicted the ATM signals from Pulse No: 83785, corresponding to counts in 8 distinct windows for channel 2, retrieved from JET database. The Neutral Beam Injector (NBI) was the only heating power used during this discharge, launched in the time period t = 8s–16s. This justifies the increase in number of counts for all channels in that time window [3]. As expected, the number of counts is inversely proportional to the correspondent energy window, once the presence of gamma-ray is very limited, due to the low heating power used.

CONCLUSIONS

Different real-time algorithms were developed and implemented for both FPGAs and MARTe application of the new DAQ system, installed at JET hard X-ray and gamma-ray profile monitor. The FPGA algorithms were firstly tested in laboratory, then at JET with radioactive sources, and finally with plasma during JET experiments. The processing algorithms for FPGA (sections 2.1 and 2.2) were essential during the phase tests without plasmas due to the low activity of the used sources. The events selection algorithm (section 2.4) was used to store just the acquired pulses for post-processing and real-time processing validation.

The algorithm for ramp-like pulses (section 2.2) was the preferred solution to process in realtime the acquired data from diagnostic detectors. It is capable to overcome the limitations associated with the larger pulses, enhancing the SNR, and calculate in real-time the energy of corresponding pulses in a range from ~200keV to ~10MeV. This was the default mode used during JET experiments, allowing to produce continuous spectra for the 19 channels between discharges. Foreseeing improvements on the detectors path, a very-fast sampling rate could be used, for instance by replacing the digitizer modules' ADCs with the compatible 400 MSPS solution or by interleaving channels. In this case the developed parallelized processing method (section 2.3) will be requested. Moreover, the novelty introduced by the parallelized algorithm can also play an important role in future spectroscopy

diagnostics to cope with the ultra-high sampling rates (GB range) provided by new generation of very-fast digitizer modules [20].

As expected the dedicated spectrum-module algorithm for MARTe application was capable to produce every 2ms counts in energy windows for the ATM datagram, meeting the real-time requirement of publishing data in JET ATM network. Taking advantage of the real-time network connection, future experiments will use the datagram contents for controlling the JET LHCD deposition before the main heating phase. Another foreseen application is the real-time correlation between the measured hard X-rays, resulting from runaways, and the beginning of disruptions [21].

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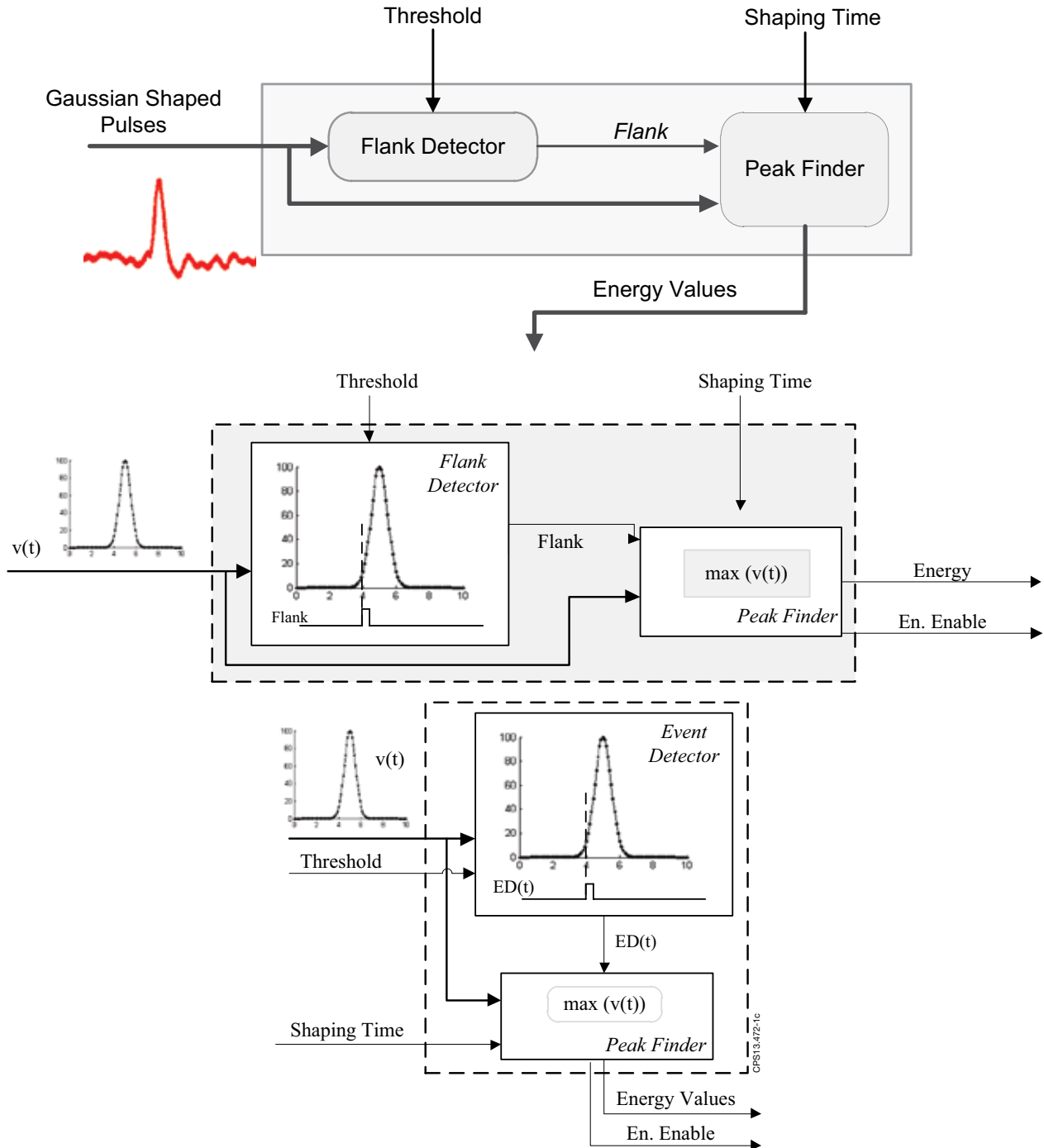
Figure 1: Schematic representation of the real-time algorithm implemented at FPGA's to determine the amplitude of Gaussian shaped pulses. The pulse amplitude is proportional to the energy of the corresponding photon that interacts in the detector.

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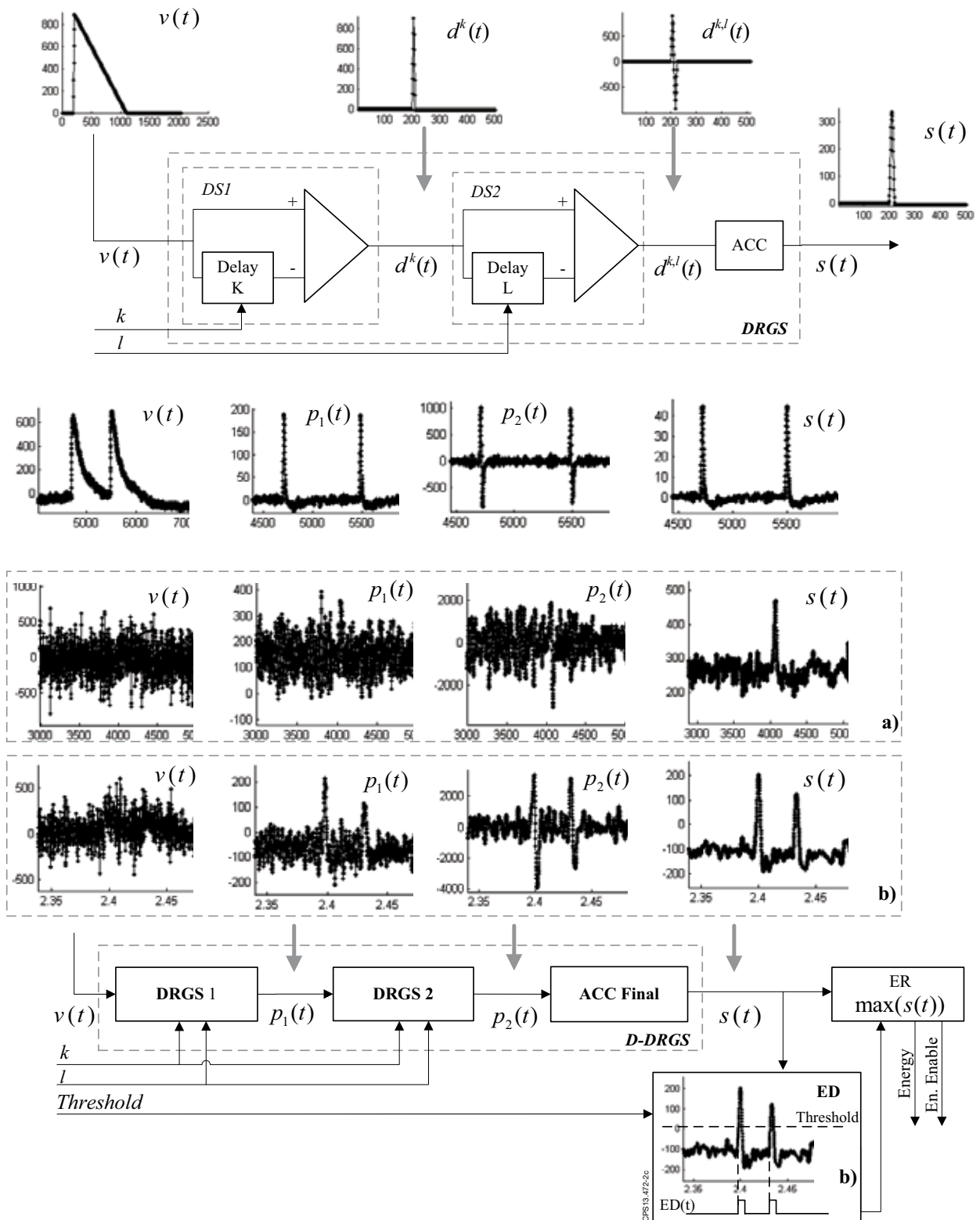
Figure 2: Schematic representation of the DRGS algorithm based on a trapezoidal shaper and adapted to ramp-like signals. By removing the HPD stage from trapezoidal shaper the filtered pulses are similar to Gaussians instead of trapezoids. This filter allowed to reduce the shaping time considerably, avoiding superimposed pulses.
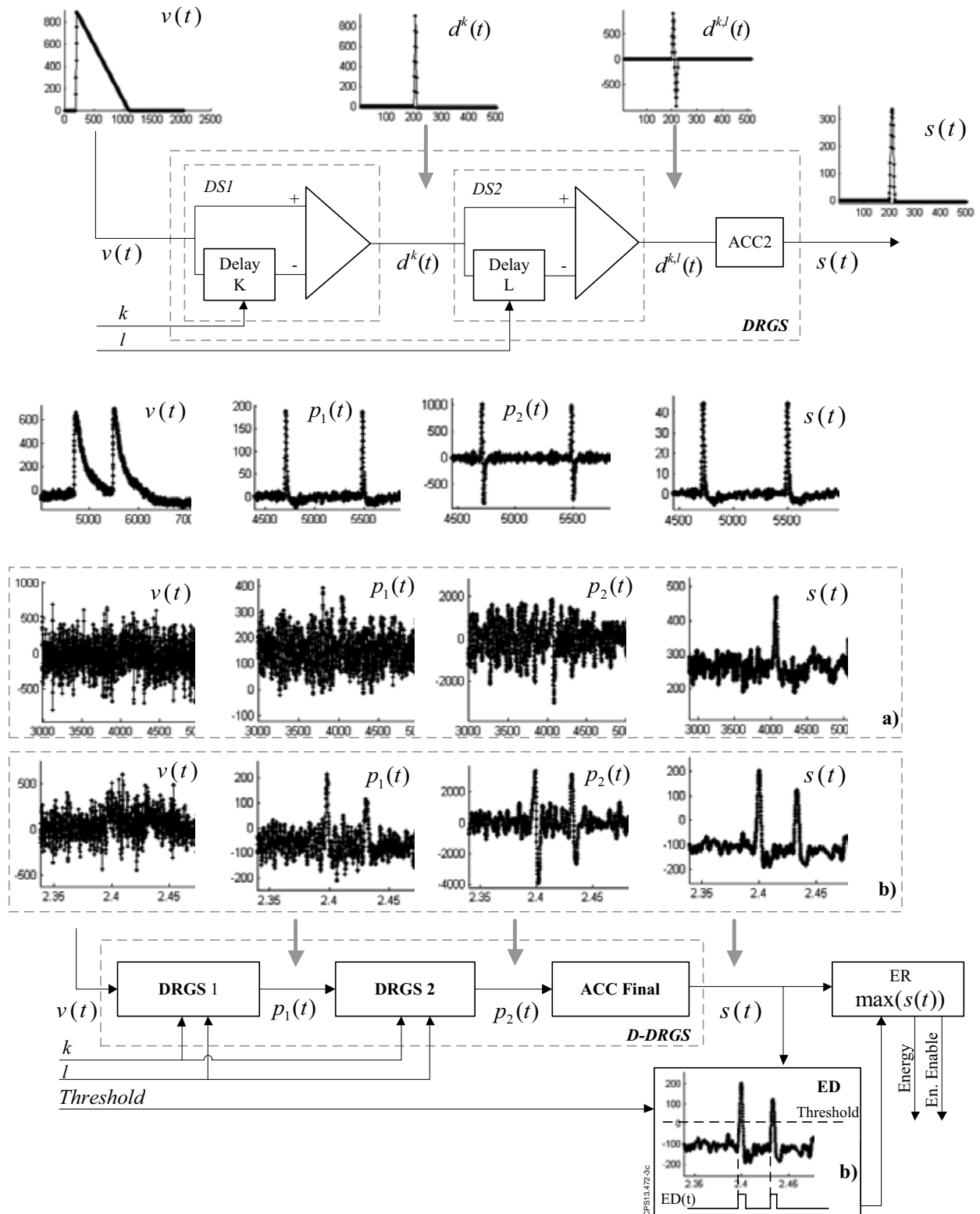
Figure 3: Schematic representation of the real-time algorithm, based on a trapezoidal shaper and adapted to CsI(Tl) detectors signals. Due to the poor SNR ratio presented by the CsI(Tl) signals, associated with long decay time pulses, the best results were achieved when DRGS was applied twice followed by a final ACC (D-DRGS). The signal a) evolution, from channel 17, highlights the importance of applying two DRGS stages for low energy pulses, since the pulse is still embedded in noise after the first DRGS. The signal b) evolution, from channel 13, stresses the algorithm capability in resolving pileup. The D-DRGS output (s(t)) is truncated to the 16 most significant bits, converting it to a 16–bit word, as required by the next FPGA stage.
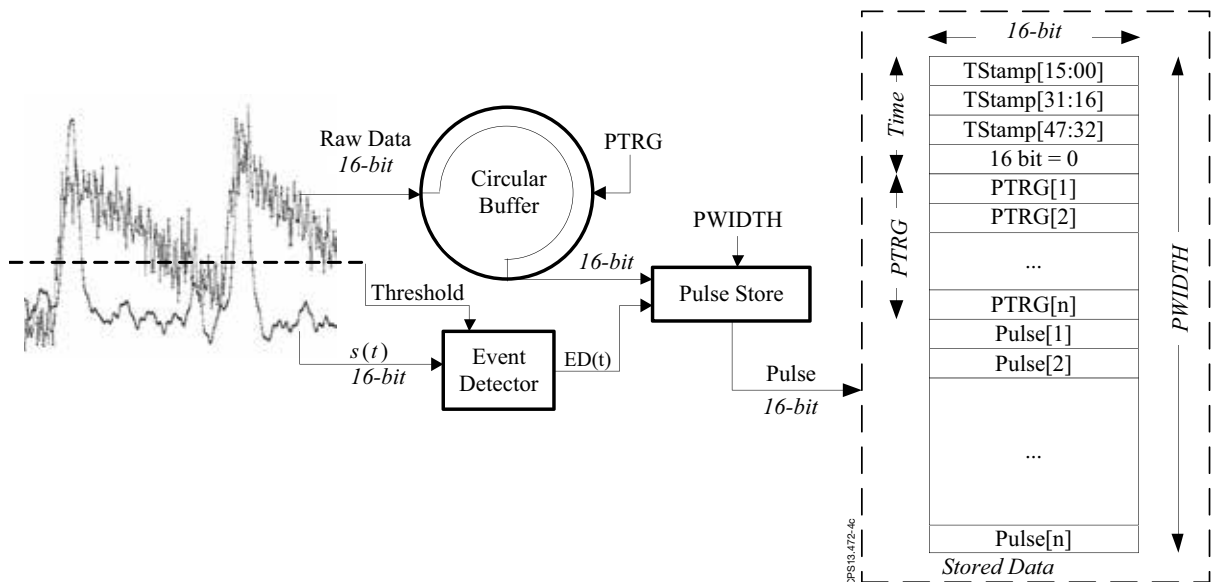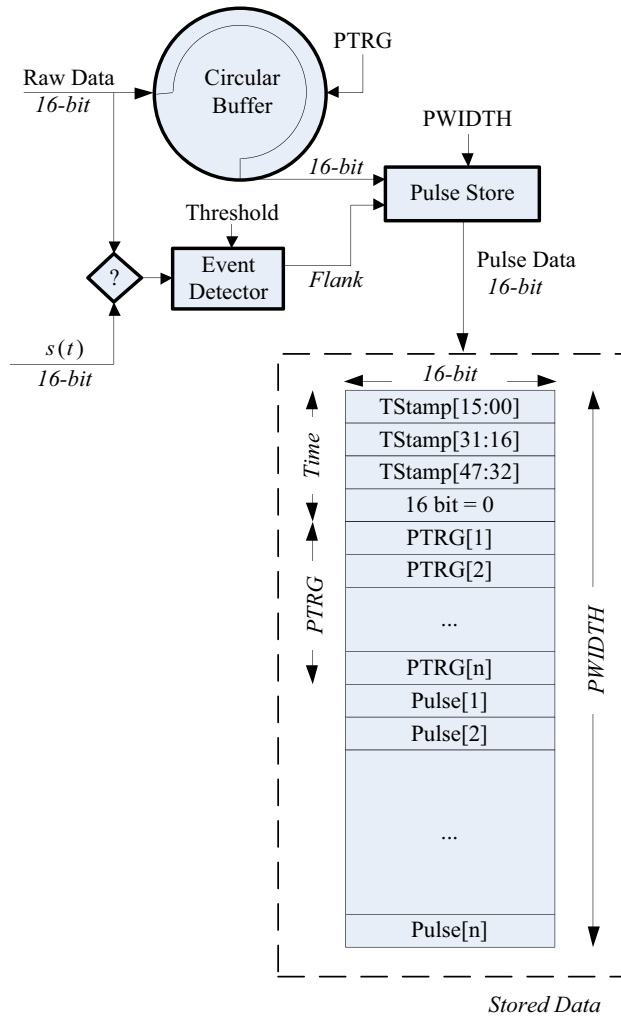
Figure 4: Schematic representation of the real-time event selection algorithm adapted to CsI(Tl) signals. Considering the diagnostic poor SNR, the ED is applied to the filtered signal instead of to the input data. When a trigger event occurs in the filtered signal, a predefined number of samples (PWIDTH) are stored with the corresponding pulse and the associated time-stamp.
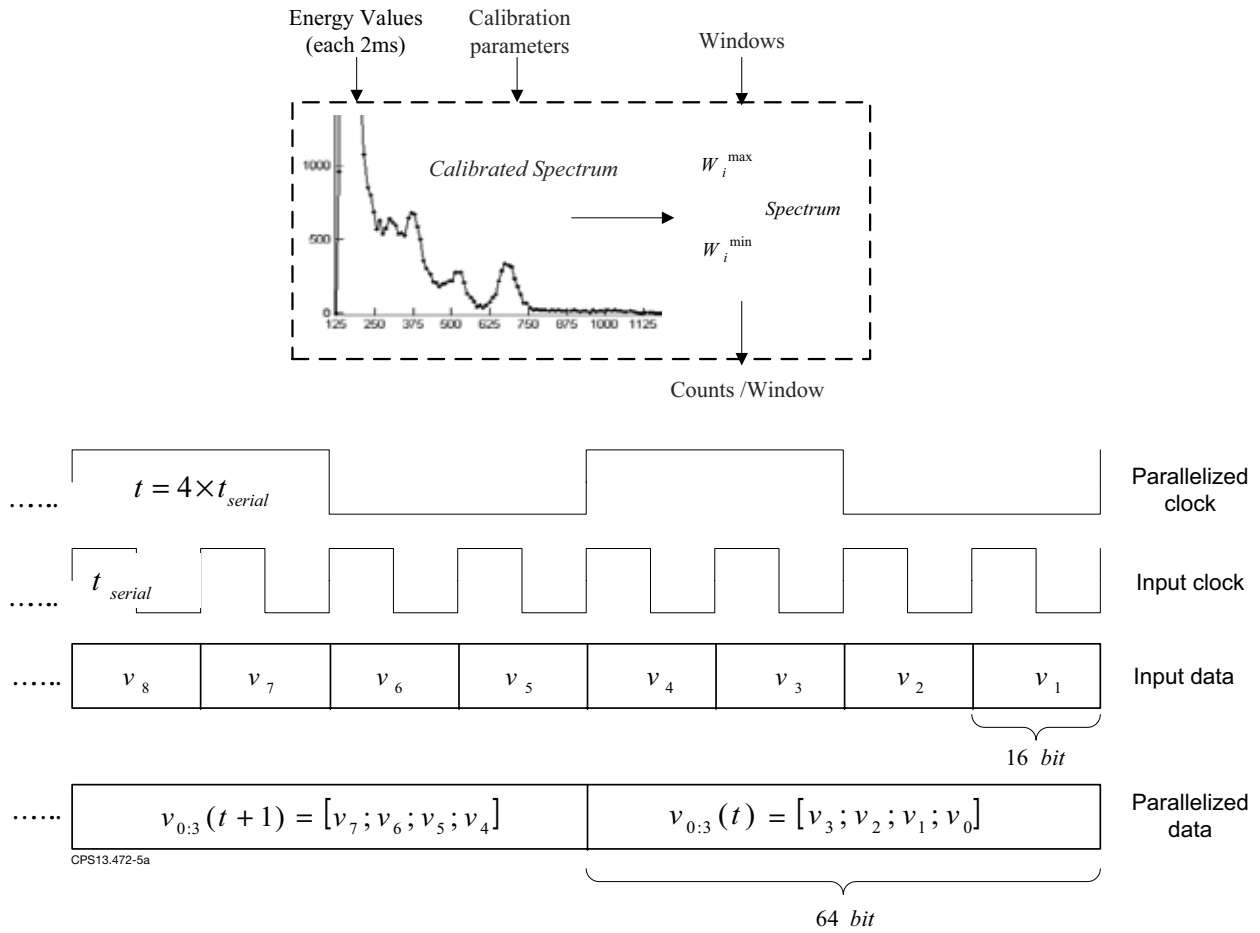
Figure 5: Schematic representation of the spectrum-module, delivering the counts to be published in the ATM network. The spectrum-module allows to build real-time calibrated spectra for a single channel, and determine from those spectra the total counts in predefined energy windows.
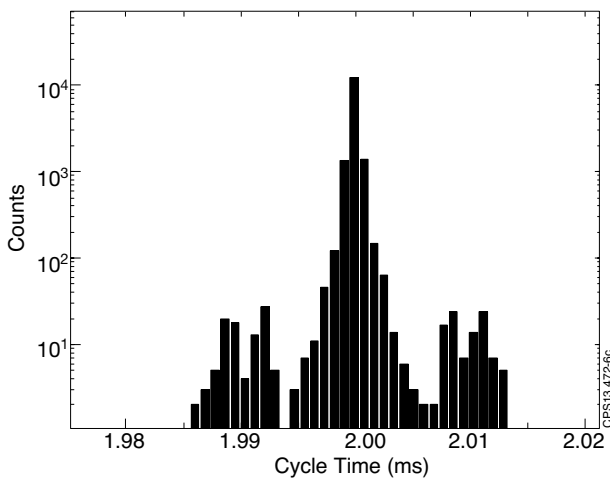
Figure 6: The overall cycle time measured by MARTe during the discharge. The system is running in a Intel[®] Core[TM] 2 Duo with Linux[®], kernel version 2.6.35.9., and with an isolated CPU for MARTe's real time thread.
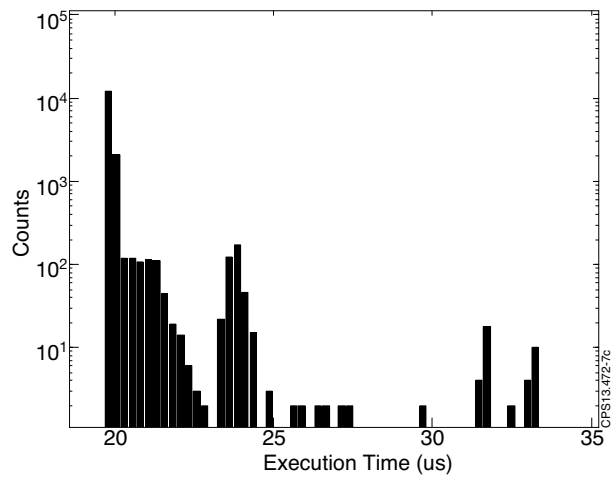

Figure 7: The spectrum-module measured execution time. The time necessary to perform the spectrum-module in each overall MARTe cycle time is about 20μs, with a maximum jitter of 14μs, running in a Intel[®] Core[TM] 2 Duo with Linux[®], kernel version 2.6.35.9.
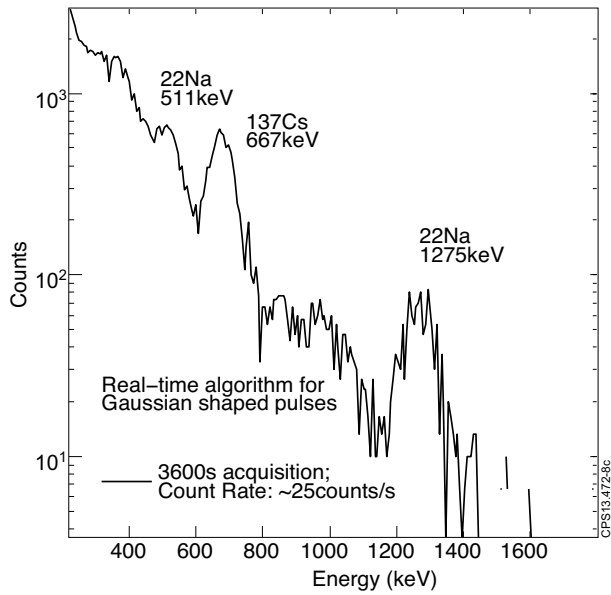
Figure 8: Spectra obtained with real-time algorithm at FPGA for Gaussian shaped pulses. An analog shaping amplifier (ORTEC 670) was used with gain10 and 10µs of shaping time. Data was acquired at 5Msamples/s.
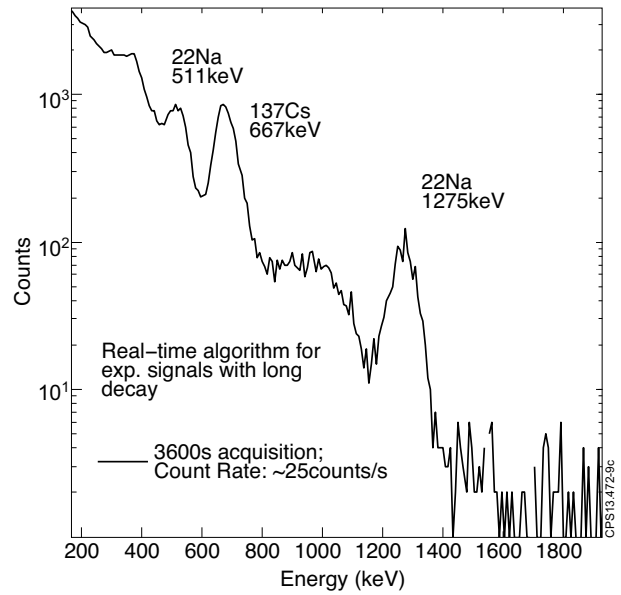

Figure 9: Spectra obtained with real-time algorithm at FPGA for ramp-like pulses. The shaping time used was 19µs and data was acquired at 2.5Msamples/s.
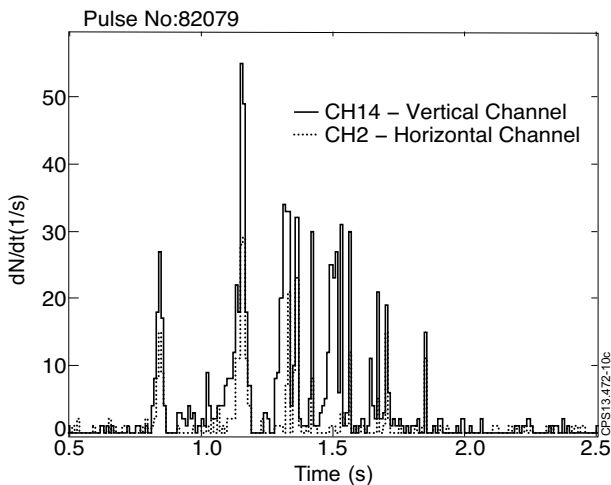

Figure 10: Spikes from runaways observed in Pulse No: 82079 discharge during ramp-up by channels 2 (horizontal channel) and 14 (vertical channel). Similar results were observed by other JET diagnostics [19].
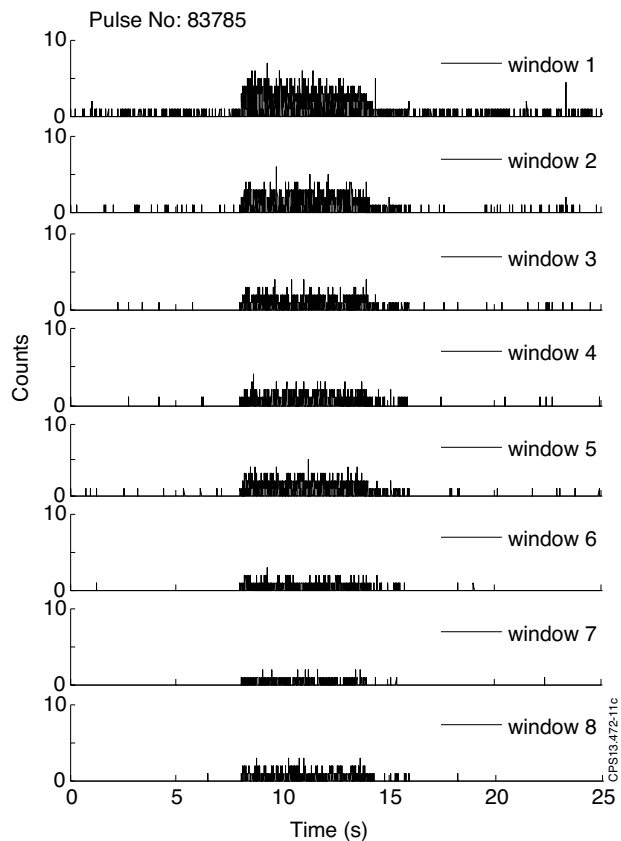

Figure 11: ATM signals stored in JET database, obtained for Pulse No: 83785. The signals correspond to counts in eight distinct windows for channel 2. The windows interval, starting from the top to the bottom are: 125–225keV; 225–300keV; 300–375keV; 375–450keV; 450–720keV; 650–790keV; 1200–1350keV; 1550–2350keV.

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