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ABSTRACT
At JET a unique 8-coil antenna system has been implemented to study the plasma instabilities due to fast-ion interactions with Alfven Eigenmodes in support of ITER. The present system has a single amplifier with a power of 5kW that is controlled by ageing electronic modules. This single amplifier was driving all eight different in-vessel antennas, with only +/– (0^o or 180^o) control of relative phase between the antennas, and with only a common single frequency sweep. The new system is comprised of eight individual 4kW amplifiers to drive the antennas, increasing the total system power to 32kW. The existing function generator and control electronics are replaced by National Instruments FPGA-based cards and PXI Express platform. This unit will control all eight amplifiers in real-time and is also synchronized with the JET system-wide 1MHz reference clock. The different functions of the digital control unit are to generate the amplifier drive signals with the desired frequency and phase, and to control the gain of all eight amplifiers. This paper will cover the system architecture, the initial test results and the advantages of this new system compared to the older system.

1. INTRODUCTION
JET has identified burning plasma research and development as a primary mission to support ITER. More specifically, required capabilities include a burning plasma start up predictive capability, burn control and optimization capabilities, more advanced burn diagnostics and investigating collective instabilities on self heating.

A new unique diagnostic was constructed at JET to make detailed measurements of magnetic field line oscillations, known as Alfvén waves. The diagnostic, known as Toroidal Alfvén Eigenmode (or TAE) antennas, consists of two sets of four antennas. With this diagnostic, JET is the fusion facility best equipped to study and interpret interaction between Alfvén waves and alpha particles, such as helium nuclei produced in fusion reactions. From computer simulations it is believed that the interaction of Alfvén waves and alpha particles plays a significant role in the confinement of the alpha particles and in the overall stability of plasmas [1].

2. CURRENT SYSTEM AND LIMITATIONS
The current diagnostic to study plasma instabilities in the Alfvén frequency range (10-500kHz) consists of one Bonn amplifier that provides RF currents to 8 in-vessel antennas. The Bonn amplifier is controlled by ageing electronic modules that were developed in the 90's. The system has several limitations and problems:

- Only a single excitation frequency is available - Only 0^o or 180^o relative antenna phase shifts are possible
- Only 4 antennas excited at a time limits the mode spectrum
- Aging amplifier and decreasing reliability
- Maximum currents of 6A can circulate in the antennas due to amplifier/transmission line and feedthrough limitation, leading to weak excitation in the plasma core

- INCAA modules for synchronous detection have maximum bandwidth of 500kHz and additional modules are not available

3. UPGRADE GOALS AND REQUIREMENTS

Improving the present system reliability, increasing its control capability, expanding its frequency range of operation and maximising the antenna current will provide JET with one of the best diagnostics to study the AEs towards ITER.

The first phase of the upgrade plan is to:

- Replace the old amplifier with 8 new amplifiers to independently excite 8 antennas at a time
- Maximise the antenna currents within the feedthrough limits throughout the 20-500kHz frequency bandwidth with the aim of 10kHz–1MHz
- Set arbitrary phasing (0^o up to 180^o) for each of the 8 antennas
- Increase the overall reliability of operation by installing a new digital control system, protection and control electronics

The second phase is to:

- Develop and install a new digital synchronous detection system
- Extend the operation of the control system to allow 2 frequencies of excitation
- Extend operating frequency into MHz range

The single 5kW tube Bonn amplifier is to be replaced with eight 4kW solid state class D power switching amplifiers, one for each in-vessel TAE antenna. These amplifiers are immune to reflected power throughout the frequency bandwidth 10-1000kHz. They will also provide an increase in total system power from 5kW to 32kW, as well as improve the distributed power coupling and reliability. Specific low pass filter modules will be installed at the amplifiers output in order to getpure sine plasma excitation within the specified frequency bands.

Upgrading the ageing function generator and control system to a new digital FPGA-based control system will add real-time arbitrary phase control during frequency sweeps between antennas and allow more than one drive frequency, adding the capability to study traveling modes. The new system will also include amplifier gain control through a feedback loop referenced to programmed antenna current profiles, and CODAS (the JETControl and Diagnostic System) integration for synchronization, triggering, gating, and fault tripping.

The remaining upgrades consist of adding a transformer at the Torus Hall link box to move the present transmission line resonance from around 250kHz up to 450kHz, potentially developing specific matching units for each transmission line and developing a digital synchronous detection system.

3.1 DIGITAL SYSTEM REQUIREMENTS

The digital control system is to control the new Politron amplifiers in real-time. Before a plasma pulse, parameters such as the amplifier reference current waveform and phase difference between amplifiers will be loaded onto the digital control system that is synchronised with the JET system. Once the JET pulse starts, amplifier frequency, voltage and current at the feedthrough, and trip signals will be sent every 1ms to the control system. These will be processed in real-time to safely control the amplifiers frequency and current.

More specifically the main functions of the digital control will be to:

– Control the amplifier RF frequency by applying the frequency sweep characteristics coming from the AELM (Alfvén Eigenmode Local Manager) and to generate the RF frequency signal (square wave) for all 8 amplifiers
– Provide arbitrary constant phase control between the 8 driver channels
– Achieve waveform phase resolution of 1 degree or better
– Control the amplifier gain and generate the amplifier gain control signal in order to control the antenna current, minimise its ripple and maintain a permissible amplitude
– Generate the reference signal for the synchronous detection systems (INCAAS)
– Manage the overall trip signal coming from the trip module and also generate its own trip signal and send it to the trip module

In total 22 input channels are needed for various analog inputs, clock and trigger gating control, trip signal and parameter data transfer. These inputs need to be processed by the new digital control system and output to 19 channels; 8 analog outputs for amplifier gain control, 8 drive frequencies for the amplifiers, two frequency reference channels for synchronised detection electronics and an output trip signal in case of control system malfunction. [2]

4. TECHNOLOGY OVERVIEW

PCI eXtensions for Instrumentation (PXI) is a rugged PC-based platform that offers high-performance solutions for measurement and automation systems. PXI is governed by the PXI Systems Alliance (PXISA), a group of more than 50 companies chartered to promote the standard, ensure interoperability, and maintain the PXI specification. PXI Express (PXIe) was added to the PXI standard in order to facilitate higher bus bandwidth in order to meet more intensive application needs. A PXI system is composed of the chassis, system controller, and peripheral modules. The chassis contains the PXI backplane and timing and triggering buses for applications requiring precise synchronization. The controller runs an operating system (Windows, Real-Time or Linux) and can either be embedded in the PXI chassis, or external to the system. Finally, there are an abundance of peripheral modules from National Instruments (NI) and other vendors that provide the system with I/O for any type of application.

PXI Express was designed to deliver a high degree of synchronization. PXIe maintains the 10MHz PXI backplane clock as well as the single-ended PXI trigger bus and length-matched PXI star trigger signal provided by the original PXI specification. PXI Express also adds a 100MHz differential clock and differential star triggers to the backplane to offer increased noise immunity and synchronization accuracy of 250ps and 500ps of module-to-module skew, respectively.

With additional timing and synchronization modules, advanced multidevice synchronization can be implemented by using the trigger bus, star trigger, and system reference clock features of PXI. Through shared timing and synchronization, the accuracy of measurements can be vastly improved, advanced triggering schemes can be applied, or multiple devices can be synchronized to act as one for extremely highchannel-count applications.

The FPGA-based hardware modules are based on NI Reconfigurable I/O (RIO) technology. This technology is based on 4 components: a processor, a reconfigurable field programmable gate array (FPGA), modular I/O hardware and graphical design software to program the FPGA. Together these components enable the creation of custom hardware circuitry with high performance I/O and unlimited timing, triggering, and synchronization flexibility.

NI FlexRIO FPGA modules feature PXI Express devices with Xilinx Kintex-7 FPGAs, onboard DRAM, highperformance NI application-specific integrated circuits (ASICs), and an interface to NI FlexRIO adapter modules that provide I/O to the FPGA. These adapter modules interface with NI FlexRIO FPGA modules through a card-edge connector that routes the necessary FPGA signals to the adapter module. While there is a wide range of commercial adapter modules, the open platform allows for any user to develop custom FlexRIO adapter modules to suit their applications.

5. NEW SYSTEM ARCHITECTURE

The following schematic showcases the new system architecture where the "Master Drive" refers to the amplifier digital control system. The RF frequency generation for the digital control system functions by reading a voltage from AELM, converting the voltage to the desired frequency, and outputting a square wave to the new amplifiers.

The National Instruments proof of concept includes a real-time PXIExpress Controller and synchronized frequency and phase generation up to 1MHz using a NI FlexRIO FPGA Module together with a 1Gbit/s digital adapter module and an analog input module for frequency control. A timing and synchronization module provides phase locking with the JET system 1MHz clock and provides a 500MHz clock to the digital adapter module (which uses double data rate generation to achieve the 1 Gbit/s update rate). LabVIEW Real-Time on the controller is also used for amplifier gain and interlock control.

The most challenging requirement was generating an RF signal for each amplifier that provides real-time arbitrary phase control (0o up to 180o) based on signal frequency sweep characteristics coming from the AELM every 1ms. This requirement involves ensuring a smooth transition between consecutive commanded frequencies while maintaining a constant phase relationship between channels. Figure 3 shows three channels with different phase offsets switching from one frequency F1 to another F2 while maintaining a constant phase relationship. The square wave generated also requires a phase resolution of 1 degree. To achieve this phase resolution at a 1MHz operating frequency for a square wave, the system requires a minimum update rate of 360MHz. Proposed solutions include generating an analog signal with a 300-500MHz arbitrary waveform generator. With 8 channels, this solution would not be very cost effective and a large amount of data would need to be synchronized and transferred over the bus. Instead, an FPGA-based solution would bring the waveform generation closer to output terminals (removing any bus bottleneck) by permitting real-time generation of the exact number of samples for a smooth frequency and constant phase transition based on several parameters.

In the proof of concept, the signal generated for each channel is constructed using four numbers: time to rising edge for each channel (in samples), time to falling edge for each channel (in samples), period (in samples), and number of periods (over the 1 ms interval). This information is processed by the RT controller in realtime before it is passed to the FPGA; which then constructs the waveform for the next 1ms while ensuring the phase transition occurs at the end of a complete period. Once generated, the FPGA would send a Data Ready trigger to the RT control system for a new set of waveform parameters. The following Figure shows the LabVIEW FPGA code responsible for executing a transition to a new frequency.

Expansion to two frequencies of excitation, a phase two requirement, would be possible and straightforward. Customizable NI FPGA based technology provides a cost effective solution with the flexibility and processing capabilities to provide the real-time arbitrary phase control required for the upgrade.

5.1 INITIAL RESULTS

The National Instruments FPGA based solution achieved less than 0.5 degree phase resolution at 1MHz well within the required 1 ms update time. The actual time from when the RT system received the analog input until the FPGA sends out the Data Ready signal, indicating the waveform generation process completed, was measured to be about 50 microseconds (0.05ms). And with a 1 Gbit/s card, the phase resolution possible exceeds 0.4 degree. At the most commonly used frequency ranges well under 1MHz, this would further improve the waveform resolution and enhance the system performance.

CONCLUSION AND FURTHER WORK

The digital control system proof of concept more than satisfied the requirements provided by JET. It was proved that an FPGA-based solution is capable of achieving both phase one and phase two requirements. The NI proof of concept was provided to the Institue of Physics at the University of San Paulo in Brazil, where they have developed the digital control system, integrated the system with the JET CODAS, and performed preliminary testing with simulated amplifiers. The FPGA code was also improved to provide arbitrary phase and frequency control for all 8 antennas. The next steps are to test the master driver control with the physical amplifiers, perform final adjustments and calibration, improve the log data system, and complete the documentation for the JET specification.

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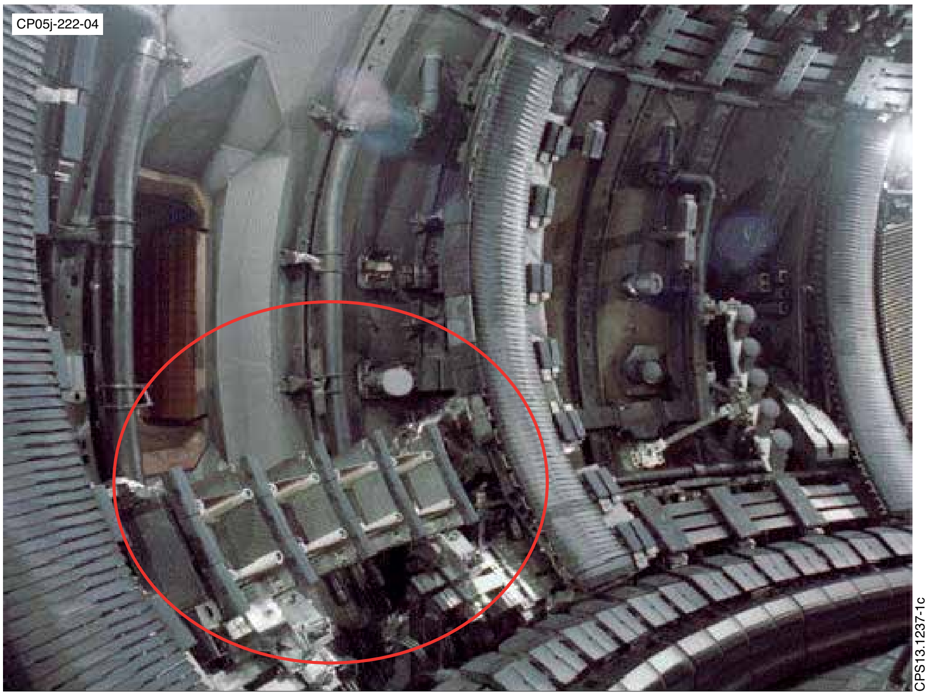

Figure 1: AE Active Antenna System on JET.

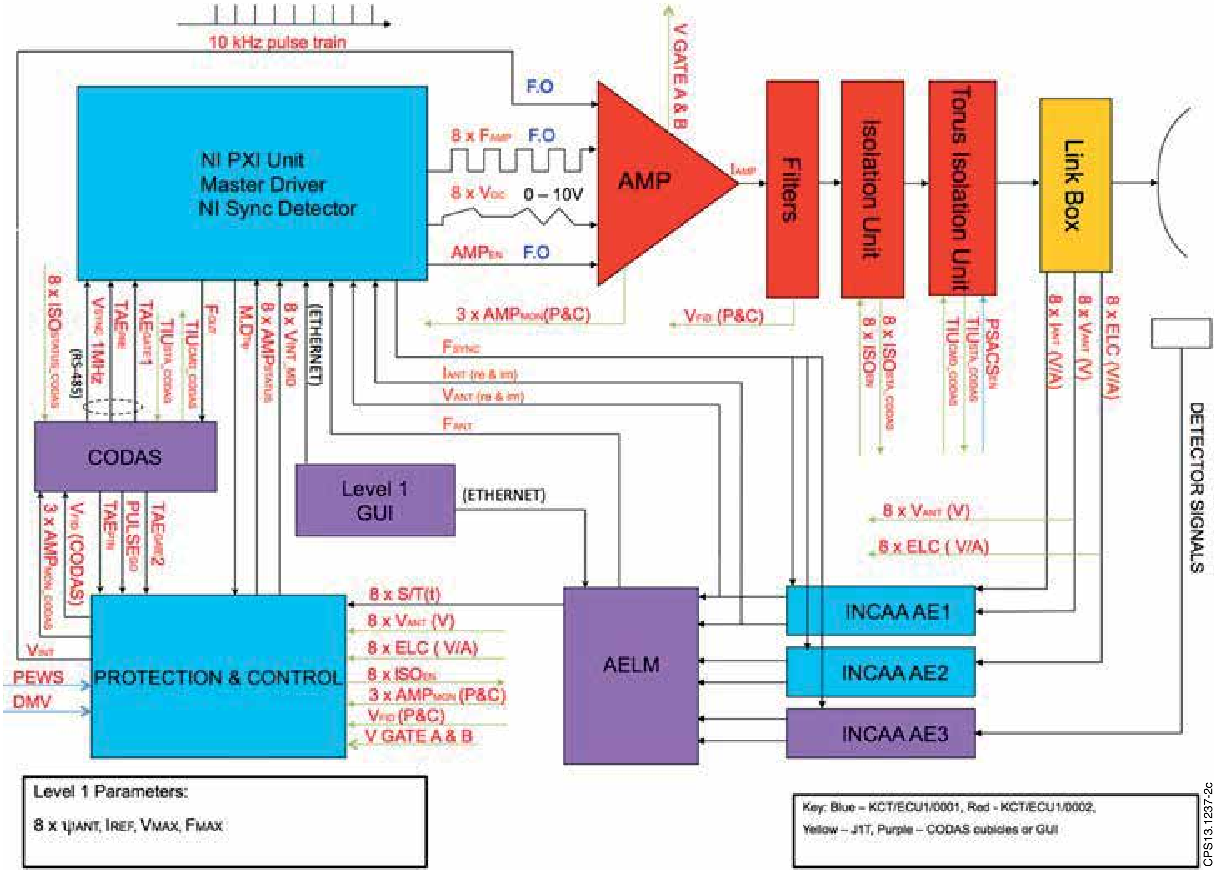

Figure 2: Overall schematic of new system

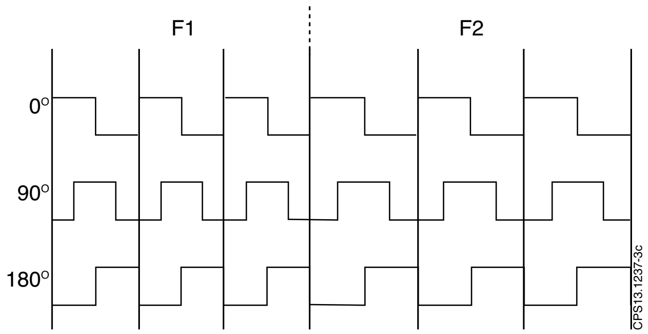

Figure 3: Maintaining the phase relative to the frequency when changing from F1 to F2 for different phase offsets

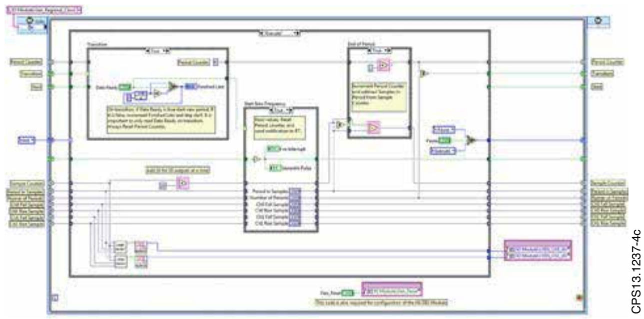

Figure 4: LabVIEW FPGA code to transition to new frequency.