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* *See annex of F. Romanelli et al, “Overview of JET Results”,
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ABSTRACT

During the last JET tokamak shutdown a new ITER-Like Wall [1] has been installed using Tungsten and Beryllium materials. To ensure Plasma Facing Component (PFC) integrity, the real-time protection of the wall has been upgraded through the project “Protection for the ITER-like Wall” (PIW). 13 CCD robust analogue cameras view the main areas of plasma wall interaction and regions of interest (ROI) are used for monitoring in real time the surface temperature of the PFCs. For each camera, ROIs will be set up pre-pulse and, during plasma operation, surface temperatures from these ROIs will be sent to the real time processing system for monitoring and preventing damages on PFCs by modifying the plasma parameters. Since 2005 a real time safety system for the monitoring of the PFCs is routinely used on the tokamak Tore Supra [2]. Based on this successful experience, a similar video and associated control system has been implemented at JET for the PIW. The overall system and the first results are presented in this paper.

1. THE PIW PROTECTION CAMERAS

The main criteria for selecting the PIW protection camera were guided by the JET hostile environment and especially:

- the robustness under high magnetic field
- the resistance to neutrons and radiations.

The chosen HITACHI black and white CCD analogue camera was used successfully in the past on JET. The simplicity of its technology makes this camera very robust under magnetic field.

The main characteristics and used settings of this camera are:

- Sensor: 752×576 pixels
- Output: 752×288 analogue Video non-interlaced
- 50 fields per second
- External synchronisation
- Exposure time: 20ms
- Standard IR cut filter removed and replaced with a near IR narrow band pass filter centered on 1 μ m with 50nm width.

The expected dynamic range is shown is shown on figure 1 with various optical apertures.

2. VIDEO DIGITIZATION AND DISTRIBUTION

The video is captured using a PLEORA iPort PT1000 frame grabber and it is sent on GigE network through an optical fiber link.

The main characteristics of the iPort are:

- Analogue video input
- GigE Ethernet output
- Sample rate: 15MHz
- Multicast capability

The iPort multicast capability allows the video distribution through a network switch to 3 different systems as shown in figure 2:

- Real Time Processing System for PIW protection
- Video capture and replay system for data storage
- Live display system for visualization in JET control room

3. THE REAL TIME PROCESSING SYSTEM

The Real Time Processing System (RTPS) has been divided into a ‘Real Time Processing Unit’ (RTPU), for surface temperature calculation, and a ‘RTPU Host’, for connection between RTPU and other systems.

The RTPU host is based on a standard industrial PC with Windows Embedded operating system.

As shown in figure 3, the choice have been made to manage 2 RTPU with one JET standard industrial PC so one standard PC will manage 2 cameras.

This choice will reduce the risks by distributing the processing units in different host computers. Then for the 13 cameras that will be installed, 7 PCs are necessary

The main functions of the RTPS are:

- Capture the camera data from Pleora iPORT modules with Intel Pro 1000 network boards and send them to RTPUs through the PCIe bus
- Get all the configuration files and values from JET Database and “Level One” then send them to the RTPUs through the PCIe bus. The configuration data are the ROI map, the dead pixel map, the Non Uniformity Correction matrix (NUC: offset and gain correction) and the calibration files that are Lookup Table (LUT) with 6 possible LUTs so 6 different materials and/or optical transmission can be managed (Beryllium, Tungsten, Tungsten coating...)
- Collect results (maximum temperature values for each ROI...) from RTPUs and send them through the JET Real Time Data Network to the Vessel Thermal Map (VTM) [3]
- Handle the central timing for synchronisation with JET pulses
- Allow ROI display for proper positioning check

4. THE REAL TIME UNIT

The RTPU design, shown on figure 4, is based on commercial Xilinx Virtex5 FPGA boards (Field Programmable Gate Array).

The on board FPGA ensures the PCIe bus and the DDR2 RAM management and of course the PIW protection functionalities.

All the parameters issued from configuration files are loaded in the on board DDR2 RAM before JET pulses.

Using Video Frame Buffer Controller (VFBC) and FIFO, the video and parameters are sent synchronously to the PIW protection engine.

Programmed under Simulink using Xilinx System Generator block set, the FPGA can manage simultaneously up to 96 ROI per camera which can have any shape.

Each ROI is defined pixel by pixel and can be split in several different areas and can overlap with others. Each pixel can belong to up to 6 ROIs.

The main functionalities included in the RTPU FPGA algorithms (schematically shown on figure 5), are:

- The PCI express bus and the on board DDR2 RAM management
- Two input FIFO interfaces for synchronisation between algorithms and RAM that are the “Image input” FIFO which handles the pixels value, vertical and horizontal synchronisation and the “Parameters” FIFO which handles the ROI and the Dead pixels maps, the NUC matrix and the used LUT for each pixel
- One “Results” output FIFO which handles all the results for each ROI
- One “Image processed” output FIFO which is mandatory for ROI map control
- The specific PIW algorithms are:
 - Dead pixels and NUC corrections
 - Neutrons impacts removal using configurable filter (Salt and Pepper 3×3 or Median 3×3)
 - Apparent surface temperature calculation using LUT (Lock Up Table) with 1 LUT per ROI chosen among the 6 stored in FPGA memory
 - For each ROI the following values are calculated : Hottest pixel surface temperature (T), hottest pixel position (x,y coordinates), uncertainty estimation using a dynamic sub ROI algorithm centered on hottest pixel (ie: Count number of pixel N in the sub ROI with value greater than X % of T, Hottest pixel is valid if $N > \text{threshold}$, N and X are configurable)
- And control registers which handles the filter selection, the dynamic sub ROI setup, the ROI highlighting...

5. THE USED COMMERCIAL FPGA BOARD

The chosen commercial board is a “Sundance Multiprocessor” PCI express SMT122T FX70T board, schematically described on figure 6, or which the main features are:

- 4 lane PCI express interface
- 1 FPGA Xilinx Virtex5 FX70T FGG665
- 2 DDR2 memory banks (256Mbytes per bank)
- 1 Serial PROM 64Mbit
- 2 Marvell 10/100/1000 Ethernet PHYs

6. TOOL FOR ROI DEFINITION

A graphical tool, running under Matlab, has been designed for creating the ROI definition file.

This tool allows the ROI drawing using JET background images. The main functionalities are:

- ROI drawing and naming with multiple sub-ROI capability
- ROI or sub-ROI deleting
- Area exclusion inside ROI
- Material (LUT) to ROI assignment
- RTPS readable file creating

7. EXAMPLE OF OBTAINED RESULTS

A preliminary result obtained using image processed displayed and recorded movies playing capabilities has been obtained and is shown on figure 8.

In this example, 6 ROIs have been used, the results are displayed in the bottom of the image:

- Maximum ROI value
- Maximum coordinate (y, x)
- ROI number of pixel (used for ROI integrity verification)
- Number of pixel in the sub ROI with value
- greater than X% of hottest pixel value (used for uncertainty evaluation)

The ROI number 0 is highlighted for control

CONCLUSION

In the frame of the JET's ITER Like Wall project (first wall in Beryllium and divertor in Tungsten), a real time protection system for these Plasma Facing Components (PFC) has been installed during last shutdown. Composed with a set of 13 CCD cameras, the protection system is based on one commercial FPGA board per camera. In the proposed approach, each FPGA board can manage up to 96 ROIs whilst for each ROI the value and position of the hottest pixel are delivered and sent to JET's VTM. The system has been successfully commissioned and validated during JET's experiments and plasma operations have been stopped by PIW system following a detection of pixels above the threshold limit. The system is now ready for routine operation and it will be particularly used for further development of high performance plasma scenario.

REFERENCES

- [1]. Guy Matthews et al Overview of the ITER-like wall project Physica Scripta Topical Issue, **T128** (2007), 137 – 143
- [2]. Philippe Moreau et al. "RF heating optimization on Tore Supra using feedback control of infrared measurements" Fusion Engineering and Design, 2007, Vol **82**, 1030-1035.
- [3]. Adam Stephen et al. "Centralised Coordinated Control To Protect The JET ITER-like Wall." ICALEPCS 2011 - 13th International Conference on Accelerator and Large Experimental Physics Control Systems.

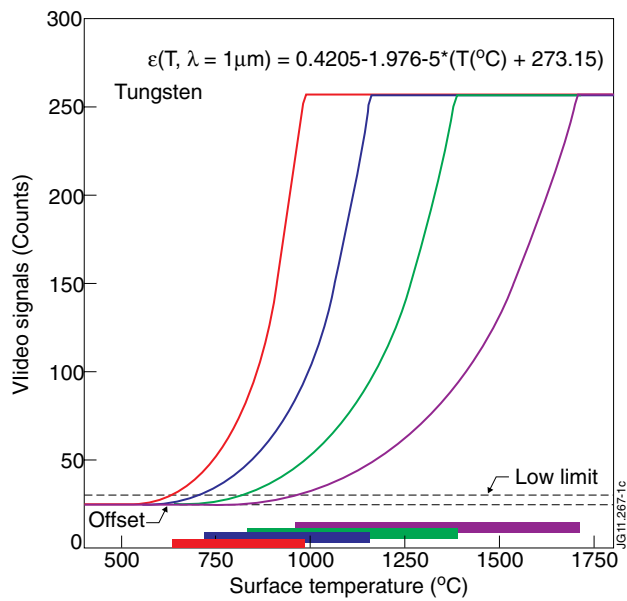


Figure 1: Hitachi camera dynamic range NIR filter: $1 \mu\text{m}$, λ : 50nm.

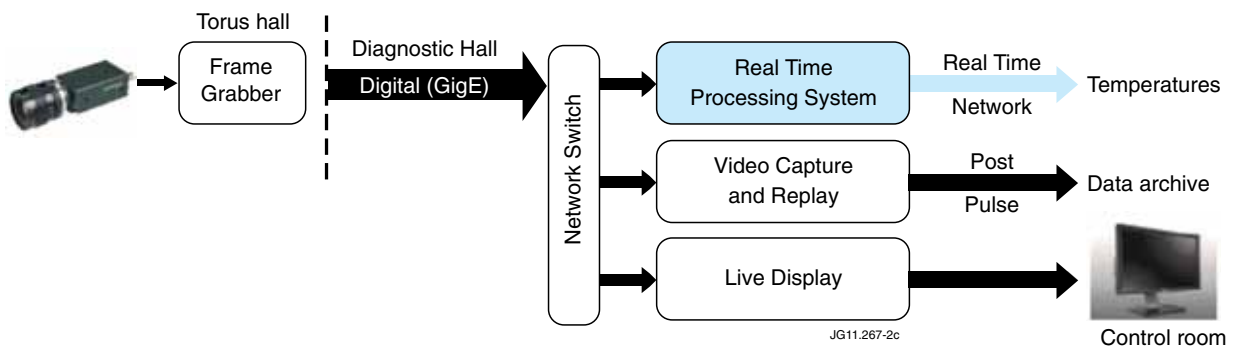


Figure 2: Video digitization and distribution synoptic.

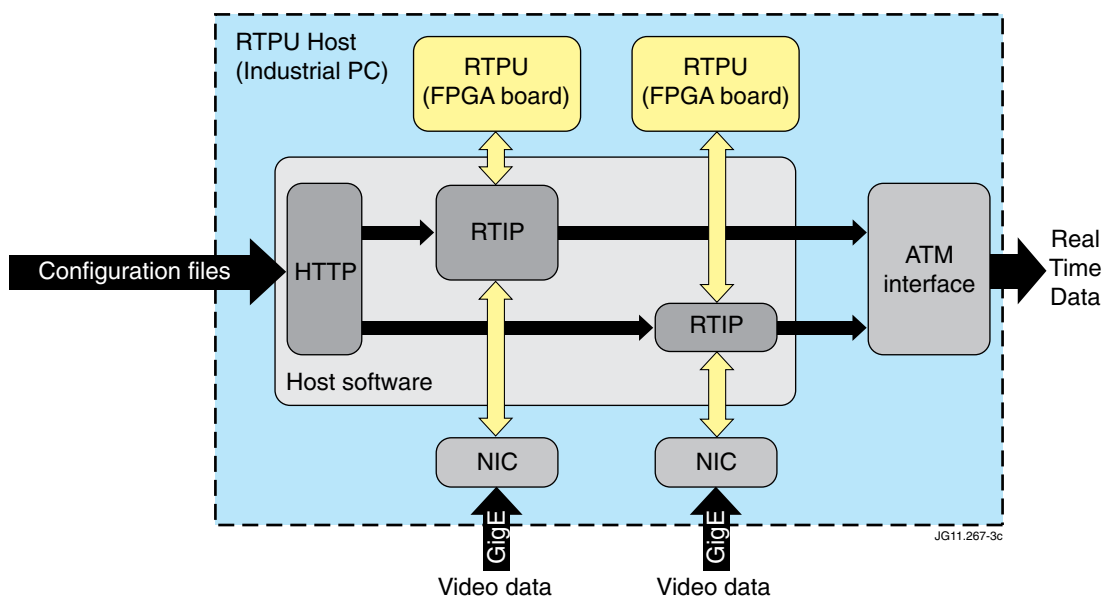


Figure 3: RTPS synoptic.

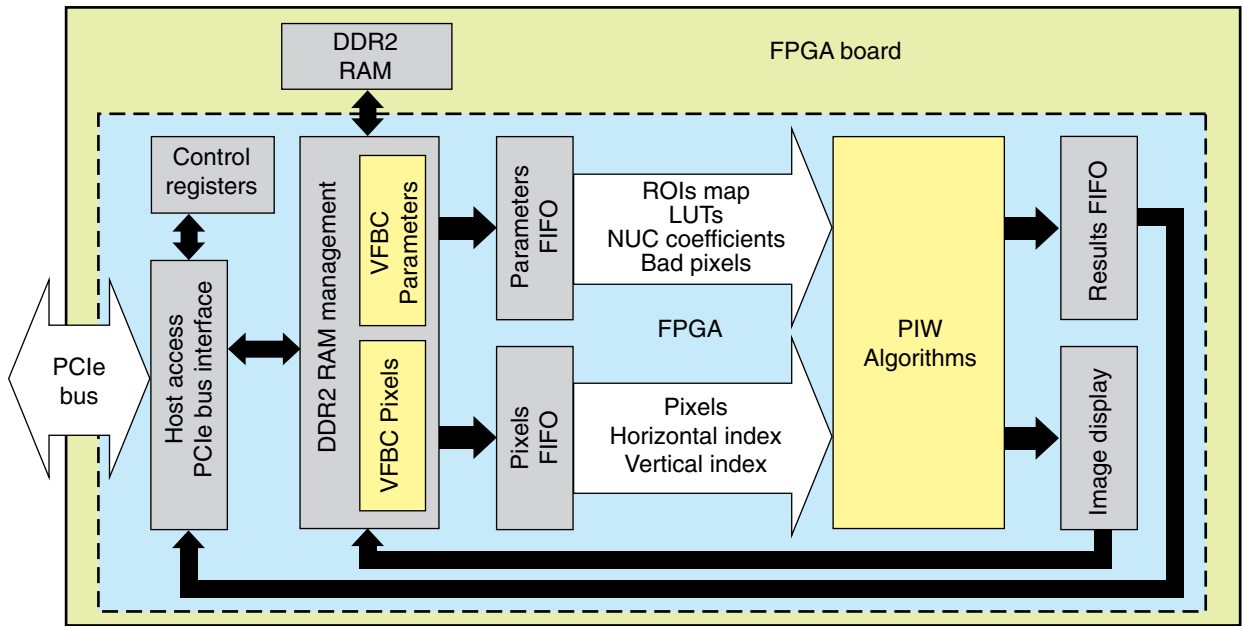


Figure 4: RTPU synoptic.

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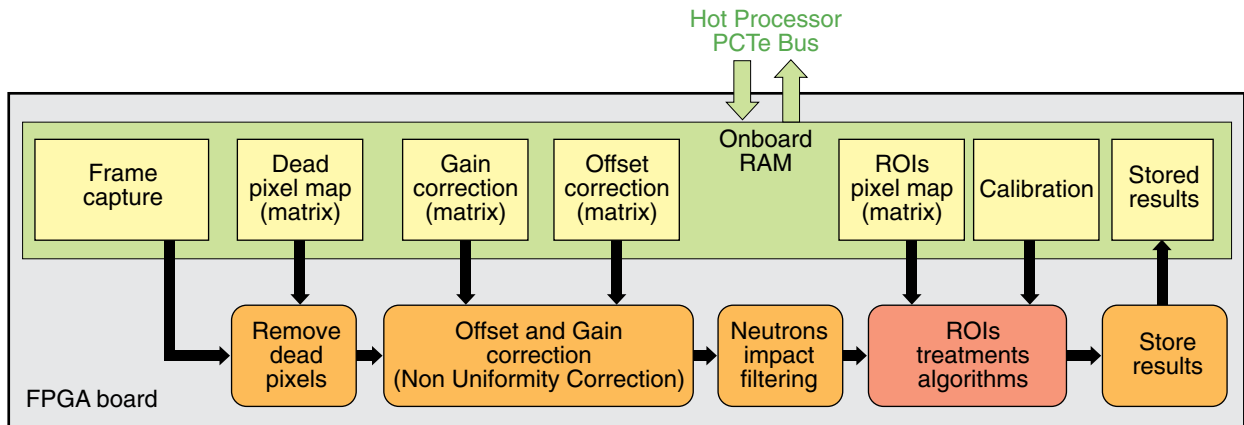


Figure 5: FPGA embedded algorithms.

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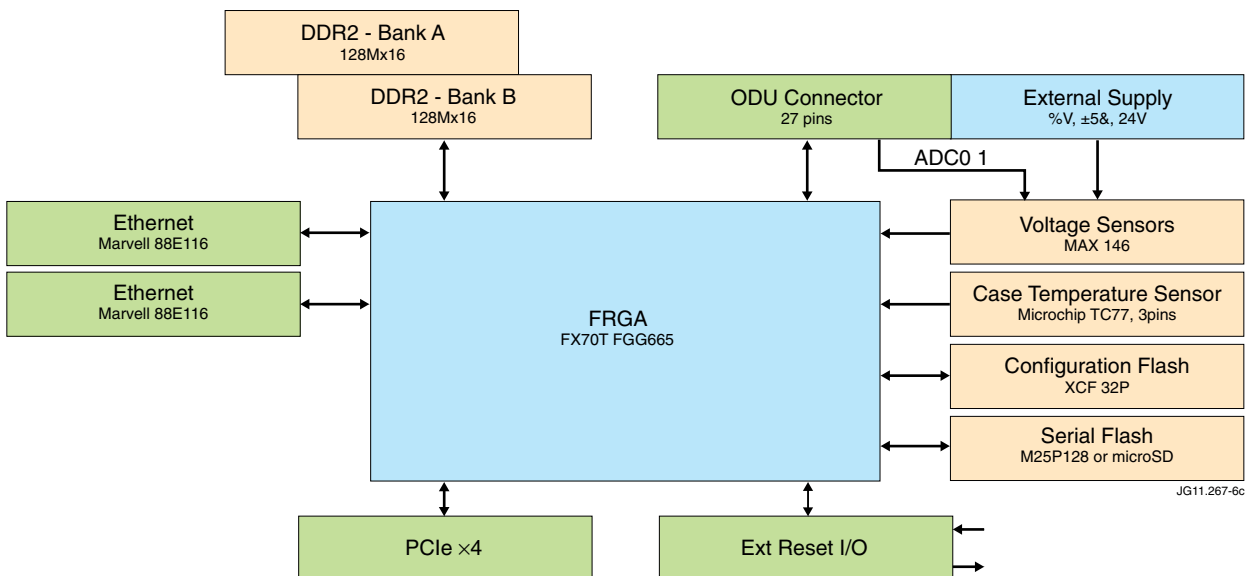


Figure 6: SMT122T FX70T synoptic.

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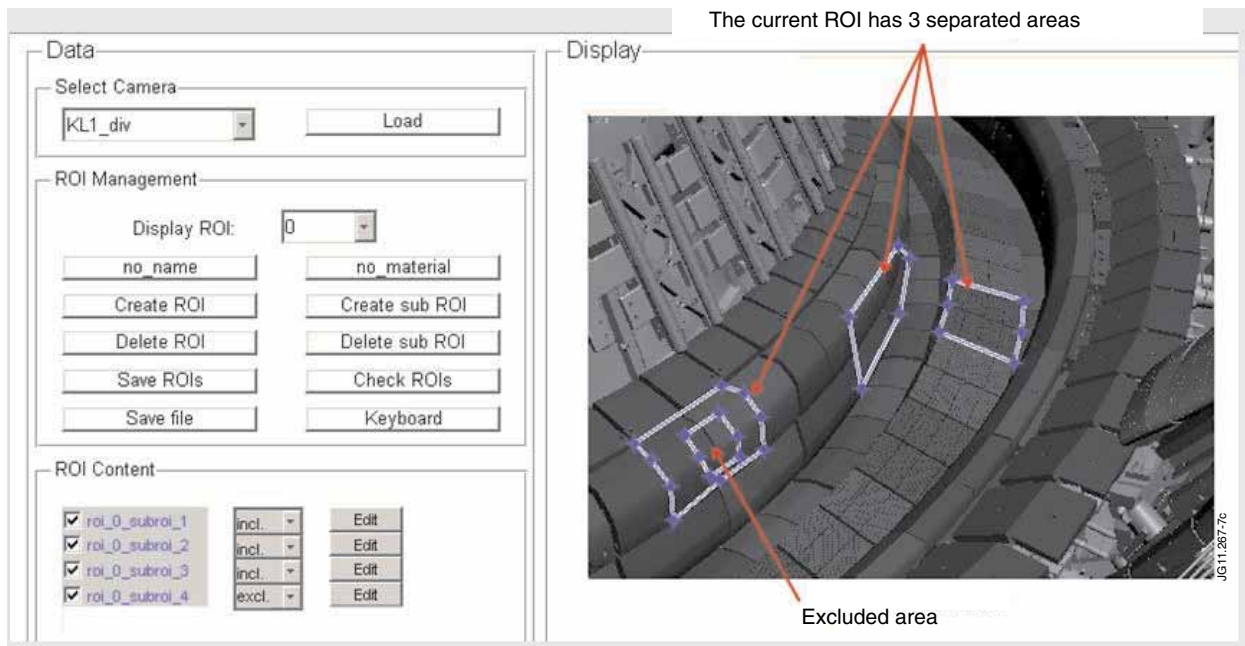


Figure 7: Software interface view.



Figure 8: Obtained results example.