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ABSTRACT

The company JEMA has delivered to the Joint European Torus (JET facility at Culham) the Enhanced Radial Field Amplifier (ERFA). This device is a high frequency, high power amplifier aimed at correcting instabilities due to fast plasma disturbances.

The system is composed of four identical units connected in series through a connection box delivering up to +/−12kV +/−5kA (60MVAr) in four quadrant operation. Each unit is composed of an input converter stage, a DC link energy storage stage, an output inverter and an output bypass (for continuing operation in case of a unit failure). ERFA works as an energy exchanger between the internal DC link capacitors bank and the JET radial field coils. The input converter compensates for power losses in the JET coils and the ERFA during operation.

The ERFA control system is fundamental for the amplifier performance to meet the speed of response required with the flexibility to achieve this for an unpredictable reference and for a wide range of load coil configurations. This paper covers the control architecture, the real-time evaluation and high speed response to the system requirements, and the fast exchange rate of data among ERFA units.

1. INTRODUCTION

The Enhanced Radial Field Amplifier (ERFA) is used to produce a rapidly changing radial field to control sudden changes in plasma parameters/position but is not required to provide 'bulk' radial field to hold the plasma in a specified position. During most of a typical plasma pulse, ERFA will not be called on to produce a significant output current. As soon as a rapid plasma disturbance is detected, the JET Plasma Position and Current Control (PPCC) system will detect the error and call upon ERFA to generate a high voltage to produce a rapid rate of change of magnetic field to return the plasma to the correct state. As the plasma may be unstable, ERFA may be called upon to reverse its output voltage rapidly, possibly between the two extremes of output voltage, several times in one disturbance and even to swing or reverse its output current; the output required of ERFA is therefore unpredictable. Once the plasma is stable, the output current from ERFA could return to value near zero. Such disturbances may occur many times in a single plasma pulse.

The topology of ERFA comprises four units with their output connected in series [1]. As shown in figure 1, each ERFA unit consists of a 12-pulse controlled rectifier converter stage fed by a matching transformer, a dc-link capacitor bank nominally charged to 3kV, an insulated Gate Bipolar Transistor (IGBT) inverter stage rated at 5kA, and an output filter to limit the rate of change of voltage applied to the load coils. ERFA is required to operate for a pulse length of 60 seconds every 10 minutes.

ERFA is designed to operate as an energy exchange system. When current is required in the load coils, electrostatic energy stored in the dc-link capacitor is transferred through the inverter to electromagnetic energy stored in the inductance of the load coils, thereby causing the dc-link voltage to fall and the load current to rise. When a reduced load current is required the process is reversed and the dc-link voltage rises as energy is recovered from the load into the capacitor. This

results in the matching transformer and converter stage being sized to overcome the system losses and not the much larger peak power flow in and out of the load.

The four quadrant operation is performed by 'H' bridge IGBT modules. This so called 'inverter stage' is responsible for amplifying the reference signal with minimum delay. A demanding requirement of the design is that the voltage reference generated by JET is virtually unpredictable. Since four identical units are used for ERFA, there are a number of operating points in which different unit switching combinations are possible. The real-time control checks the availability status of the units at every instant in terms of tolerable temperature of the most critical components (IGBTs and output filter resistors) and limits the stored energy (DC link capacitor voltage), so that the optimum switching combination can be selected. The bulk of the paper is dedicated to the description and discussion of the complex algorithms developed to this purpose.

A novel 'staggered switching' technique is also implemented. This technique is used in particular for reducing the output voltage overshoot and dV/dt, as requested by the operating limits of the JET coils.

The converter regulation in current, the Programmable Logic Controller (PLC) based overall control, the JET interface and data acquisition systems are also briefly described in this paper.

2. INVERTER REGULATION

The inverter stage in each unit consists of ten parallel IGBT 'H'-bridges. By controlling the state of the IGBTs in the inverter, each unit can apply either +3kV, 0V or –3kV to its output. By controlling the inverter stages of all four series connected units, ERFA can output between +12kV and –12kV in nine discrete levels. In case the voltage reference is lower than the possible maximum (±3kV, ±6kV, ±9kV, when 4 units are available) more than one switching vector is possible. The inverter real-time control determines which are the most convenient switching vectors in terms of keeping the DC Link Voltages at the optimum charging capability and penalizing switching in units that are at higher junction temperature.

In order to be prepared for switching as fast as possible, a digital control, basically composed of a Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA), is used to implement the inverter control algorithm. The following sub-sections define the most important stages of the inverter control algorithm.

2.1. ENDLESS LOOP

An endless loop is computed by the inverter DSP. The FPGA generates an interruption to the DSP every 50μs. In case of even interruption number, a process of anticipation to a new voltage reference (described in 2.3) is launched. It calculates offline the switching vectors for every 9 possible expected references and downloads the result into the FPGA memory.

In case of odd interruption a DC energy equalization process (described in 2.4) is evaluated. If the energy on the DC Link of a unit is well above or below the average, the inverter swaps 2 units

(highest & lowest energy), so that the output voltage is maintained, but the DC links are equalized. This operation can only be performed under certain conditions.

Before beginning any of these two processes it is necessary to make a good assessment of the energy stored in the DC Link of each unit.

2.2 EVALUATION OF THE UNIT ENERGY

In the process of anticipation to a new voltage reference and the equalization process the concept of Unit Energy is used. Additionally to the DC Link Energy, there are other important factors which need to be considered when deciding which unit to switch: The temperature or heating availability and the Switching history.

For simplifying calculations, the DC link Energy and the IGBT's Maximum Junction temperature (Tj max) are merged in one single parameter, which is generically called "energy".

The diagram below (figure 2) shows the associations. DC Link Energy is proportional to the square of the DC Link voltage. The deviation of this DC Link Energy in relation to the average is operated with the calculated junction temperature defined in ºC. The Filter Resistor calculated temperature also gets in the Tj max evaluation. A scaling is performed: 400ºC on the resistor are set as equivalent to 90ºC on the semiconductors.

Switching history is taken into consideration by penalizing the last units having switched. A correction factor adjusts the contribution of the temperature and switching history to the evaluation of the unit energy.

2.3. PROCESS OF ANTICIPATION TO A NEW VOLTAGE REFERENCE

This process is performed every even DSP interruption. Units are ranked according to the results of the evaluation of the unit energy. Depending on three parameters: the relative energy status of the unit (in relation to the average), the sign of the output current and the present output of every unit, the control determines 9 switching vectors which are stored in the FPGA. These 9 vectors are the only possible switching states resulting from a single reference change. If the voltage reference changes at any time, ERFA performs instantaneously the corresponding switching sequence already stored in the FPGA.

With a positive output current the units applying +3kV transfer the DC Link Energy to the load, the units applying -3kV recover energy from the load and the units applying 0V maintain the DC Link Energy. With a negative output current the energy flow is reversed. In any case, switching vectors for positive voltage references only consider +3kV and 0kV possible values. For negative voltage references, only -3kV and 0kV are considered. Opposite polarities in the same switching vector are not allowe . With thess rules and knowing the mentioned three parameters the process will balance the energy between the available units. Figure 3 shows the 9 switching stages generated from a given unit energy ranking, an initial unit state and a given current sign.

2.4. PROCESS OF EQUALIZATION OF THE DC LINK ENERGIES

This process looks at the energies of the 4 units and investigates if keeping the same output voltage it is possible to find a different switching vector which allows to better energy equalization. The process is performed when the evaluated energy in one or more units differ in more than 10% from the average energy.

The main difference to the process described in 2.3 is that in this case, unit switching rotations may be produced without an output voltage reference change.

2.5. CONTROL TAKEOVER

In case the output current gets to a limit value, the internal ERFA control takes over any external reference, in order to keep the output current within the defined tolerance and avoid a trip sequence. Depending on the current level, the control may set the output to 0V or to the full range (+12 or -12kV) of the opposite polarity.

The takeover current threshold and the decrement for getting back to reference are adjustable from the control interface and the limit values decrease if one or more units are bypassed.

2.6. STAGGERED SWITCHING

There is a concern in trying to reduce at maximum the stress on the existing control coils of JET. Consequently, the specification limits the output voltage overshoot and the dV/dt on the output cables. The output RLC filter has been designed for meeting the requirements above. Additionally, a staggered switching technique allows to actively further reduce dV/dt and voltage overshoot. The technique consists in avoiding that +12kV (or -12kV) are instantaneously applied. Overshoot and dV/dt are significantly reduced if an intermediate stage at +9kV or -9kV is inserted for about 100μs. This way, the filter resonant peak is divided in two portions and a flatter voltage waveform results.

2.7. HIGH FREQUENCY TRANSITION FILTER

A high frequency filter is implemented in the FPGA for transistors overheating protection. It avoids switching at higher speed than 10 kHz. If two reference transitions are received in less than 40μs, the high frequency filter ignores any new reference change for 100μs.

It is important to note that the control takes into account only the available units for all the calculations and processes described above. Operation of ERFA is critical for JET in order to avoid disruptions during a pulse. Therefore, ERFA is designed so that if a fault develops in one unit during a load pulse, then that unit can either continue to operate normally (e.g. for alarm type faults) or it can be bypassed (e.g. for trip type faults) so that the load pulse may continue using only the remaining units. If one or more units are bypassed, there is reduced output voltage capability (i.e. with reduced maximum voltage, reduced number of output voltage levels available, and reduced switching frequency).

3. CONTROL OF THE DC LINK VOLTAGE AND THYRISTOR CONVERTER REGULATION

ERFA acts as a reactive energy exchanger between the units DC capacitors bank and the JET coils. The input rectifier only needs, in principle, to compensate for the power losses in ERFA and the JET Coils.

Every unit incorporates a 12 pulse thyristor converter with 2 bridges connected in series for performing the rectifier function.

From the exposed reactive energy exchange principle, the DC Link voltage reference is variable depending on the ERFA output current. The following equation allows achieving the voltage reference for the tyristor converter.

$$\frac{1}{2} \cdot S \cdot (Vo_{DC}^2 - Vo_{DC}^2) = \frac{1}{2} \cdot L \cdot I_{out}^2 \quad (1)$$

Where:

Vo_{DC} is the dc link voltage at 0 output current.

Vo_{DC} is the dc link voltage reference.

In a second control loop, the converter is regulated for behaving as a current source. The current is set to 300A or 100A depending on the overheating capabilities for the semiconductors.

The regulation is performed by a DSP control card located in each unit. The Integration constant changes depending on the PI (Proportional Integrative controller) error magnitude and the DC current level, for avoiding overshoots, while ensuring a fast response. The DC current reference is ramped, and this is for avoiding overshoots and ensuring a soft start of the 12 pulses converter.

Complete control scheme is detailed in figure 5.

4. Operating Modes

The normal mode of operation of ERFA is as a high speed voltage amplifier. It will operate in open loop, i.e. the overall output voltage is set at one of the nine levels (+12 kV to –12 kV with +/-3kV steps) depending on the output voltage demand signal received from the PPCC system which will close the overall control loop.

ERFA accepts the output voltage demand signal as a digital signal with nine states corresponding to the nine possible output voltage levels of ERFA.

Also the output voltage demand signal can be received as an analogue signal and converted to the nine state digital input. In order to avoid excessive switching between output voltage levels, an adjustable hysteresis characteristic is applied.

The system can receive the voltage reference from an external analogue voltage waveform generator. This operating mode is similar to the PPCC analogue.

ERFA is also capable of acting as a current amplifier in closed loop control. This mode of operation has been used for local commissioning and testing.

Additionally, the system can work as a current closed loop regulator, controlled by an internal digital waveform generator (pre-programmed scenarios), very useful for commissioning and testing.

5. CONTROL MONITORING AND DATA COLLECTION

For monitoring purposes, ERFA provides a control monitoring and data collection system based on a Data Acquisition module. 10 parameters per units are recorded for each pulse at a 100kHz sampling The module performs the fast analogue to digital conversions, data temporary storage and offline transmission to the JET Control and Data Acquisition Systems (CODAS) over the Ethernet link.

6. CONTROL SYSTEM LAYOUT

The control structure of the ERFA is based on four independent Unit Local Controllers, coordinated by a Supervisor. The control architecture is based on four PLC's Central Processing Units (CPU) located in the control area of each unit and four Slave Modules in the high voltage areas. The data transmission between both areas is made through fiber optic channels.

The CPU located in unit one acts as the Supervisor of ERFA. The Supervisor is the single interface point with JET systems like Plasma Position Current Control (PPCC), Central Interlock and Safety System (CISS), Direct Magnet Safety System (DMSS), Central Timing System (CTS), Pulse Termination Network (PTN) and Control and Data Acquisition System (CODAS). It also coordinates switching of the 4 units.

CONCLUSIONS

Using appropriate control techniques an equalized energy balance between available units, as well as a fast response of the system has been achieved. The general requirements have been fulfilled in the commissioning and the proposed algorithms have been validated. The ERFA, controlled as described on this paper, is fully operational on the JET facility.

REFERENCES

[1]. D. Ganuza, D. Rendell, B. Arenal, J.M. de la Fuente, S.R. Shaw, V. Toigo, M. Zulaika, A. Arenal and JET EFDA contributors, "Conceptual Design of the Enhanced Radial Field Amplifier for Plasma Vertical Stabilisation in JET", Fusion Engineering and Design **84** (2009), 810-814

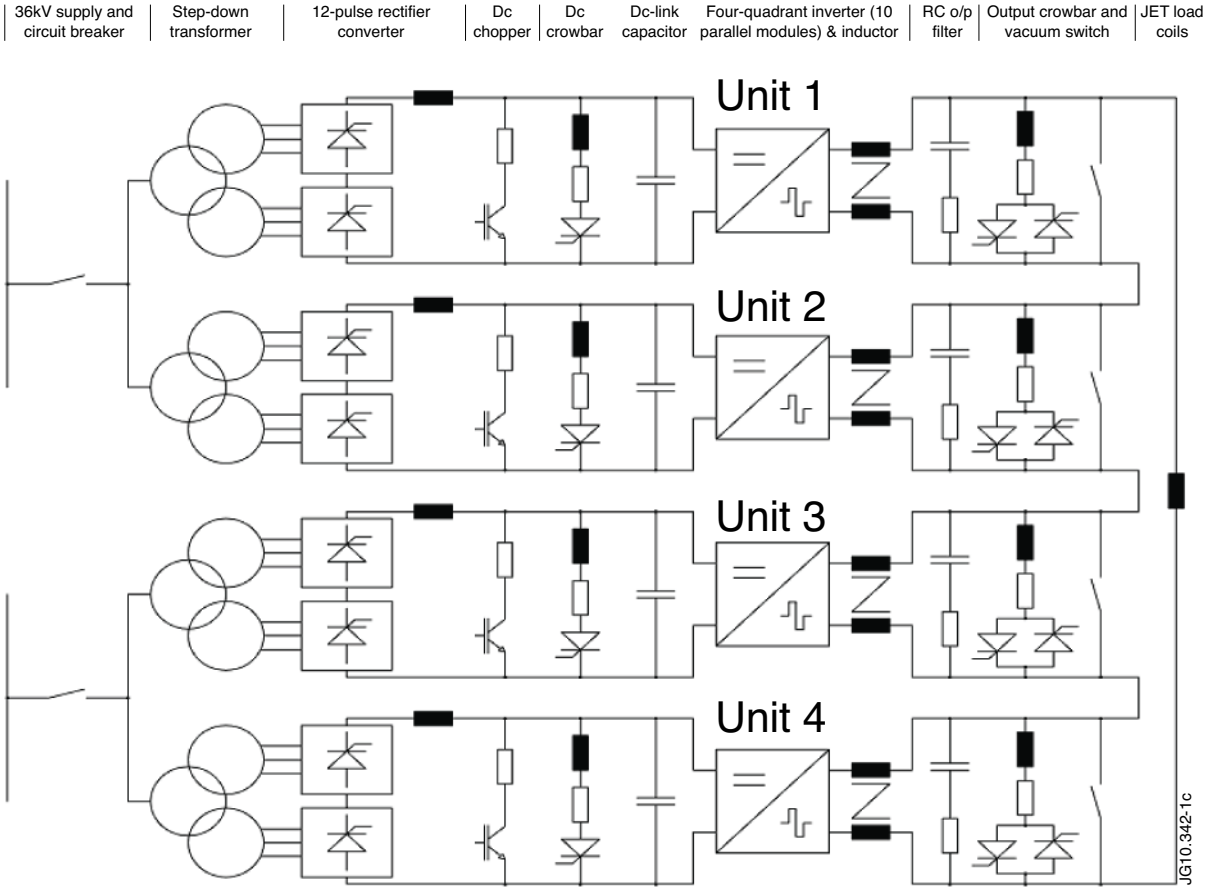

Figure 1: ERFA Single Line Diagram

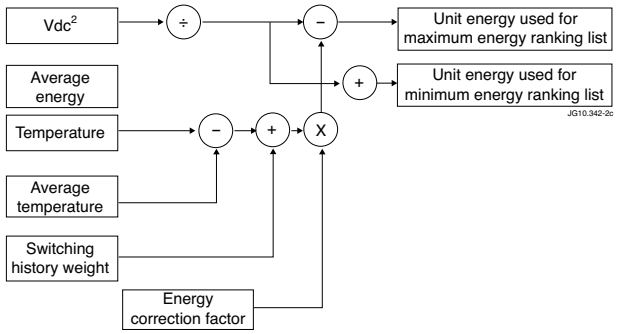

Figure 2: Evaluation of the unit energy.

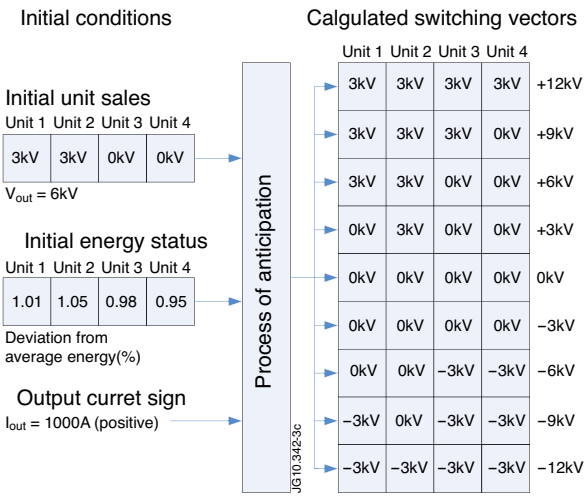

Figure 3: Example of vector generation.

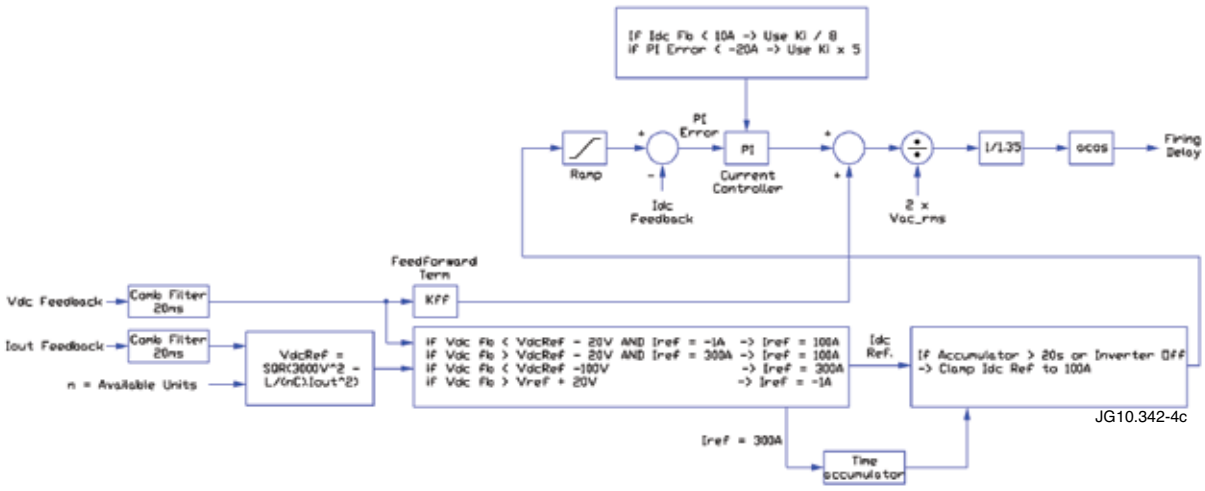

Figure 4: Thyristor converter regulation.