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** See annex of F. Romanelli et al, "Overview of JET Results", (Proc. 22 nd IAEA Fusion Energy Conference, Geneva, Switzerland (2008)).*

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ABSTRACT.
Magnetic field perturbations which break the toroidal symmetries are inevitable in tokamaks due to imperfections in magnetic field coils and to the presence of magnetic materials. Magnetic islands arising from these asymmetries can cause the appearance of locked modes which, if uncontrolled, frequently lead to disruptions. One of the main goals of the Error Field Correction Coil (EFCC) systems in modern tokamaks is to alleviate this effect by applying magnetic perturbations that compensate the natural error field at the plasma boundary. Recently at JET, performance issues and practical limitations led to the decision of replacing the EFCCs voltage amplifiers. The opportunity was also taken to reformulate and improve the controller application by incorporating it into a new real-time software framework, developing a new control algorithm and revising the time synchronization mechanism whilst maintaining essentially the same VME based hardware components. Furthermore, a new graphical user interface configuration utility has been developed mainly to accommodate the new controller's waveform generator capability of nesting waveforms and enabling simultaneous sweeping in frequency, amplitude and offset. In this paper, a global overview of the new controller application will be provided focusing mainly on the above mentioned improved elements. Preliminary results of the operation of this system during JET pulses will also be presented.

1. INTRODUCTION
Error field correction is currently employed, or planned for, in several tokamaks around the world including DIIID, Alcator C-Mod, NSTX, ASDEX-U, KSTAR, MAST and JET. It is also foreseen in the design of the ITER tokamak, [1]. Its primary use is correcting the usual, and potentially disruptive, magnetic perturbations of resonant topologies such as the m = 2 and n = 1. Also, more recent results extend the benefits of the EFCCs to the mitigation of Edge Localized Modes (ELMs) by increasing their frequency, thus, reducing their size and transient heat load at limiter surfaces whilst maintaining good plasma confinement [2]. In JET, the EFCC system can be operated in two distinct congurations depending on the required resultant magnetic topology (n = 1 or n = 2). Two Voltage Controlled Voltage Sources (VCVSs) are available for driving the four EFCCs which are physically placed in octants 90 degree apart. Either one VCVS drives all four EFCCs or, as illustrated in Fig. 1, each VCVS drives two EFCCs. The user configures the required current reference waveforms and loads the controller application's configuration using a JET standard interface called Level-1, [3]. The controller application then uses, in real-time, the current reference and the current measurement along with the VCVS output voltage to close the feedback loop by performing appropriate voltage requests. The recent substitution of the VCVSs driving the EFCCs has motivated the reformulation and improvement of a number of aspects within the real-time controller application.

2. HARDWARE ARCHITECTURE AND SYNCHRONIZATION
2.1. HARDWARE COMPONENTS
The controller system hardware is based on the previously existent VME technology. Essentially, it comprises a VME crate hosting the following modules:

- VME Programmable Logic Service (VPLS)

- VX5100 PowerPC
- MPV956
- MPV922

The VPLS is a JET specific module that provides timing information, synchronous with JET's Central Timing System (CTS), with a resolution of 1ms. The VX5100 module is a Motorola® PowerPC board with a 400MHz Central Processing Unit (CPU) and 64 MBytes of RAM. The MPV956, by Pentland®, is used both as a 12 bit (16 channel) Analog-to-Digital Converter (ADC) with ±10V input range and (8 channel) Digital-to-Analog Converter (DAC) with 0 to +10 V output range. The MPV922 module, also by Pentland®, provides up to 40 digital input channels and 32 digital output channels.

The analog driven VCVSs have an input range of ±10V linearly mapped onto an output range of ±3kV with a specified bandwidth of 75Hz and providing a maximum absolute current of 3kA.

2.2. SYNCHRONIZATION MECHANISM

The real-time controller application runs in a 200μs cycle time synchronized to an oscillator within the PowerPC board. Time stamp agreement with JET's CTS is guaranteed using equation 1 along with an adaptive algorithm that adjusts the relative skew between both clocks based on equations 2 and 3, where the j index indicates quantities updated at the VPLS/CTS rate of 1kHz and the k index indicates quantities updated at the local 5kHz PowerPC oscillator rate. In these equations, t_k is the time stamp, t_j^{VPLS} is the time given by the VPLS module with a 1ms resolution, χ_j^{corr} is the adaptive correction factor and tMeas represents a time measurement using a high resolution CPU counter.

$$t_k = t_j^{VPLS} + \chi_j^{corr} \times (t_j^{Meas} - t_j^{Meas}) \quad (1)$$

$$\chi_j^r = \frac{\Delta t_j^{VPLS}}{\Delta t_j^{VPLS}} = \frac{10^{-3}}{t_j^{Meas} - t_j^{Meas}} \quad (2)$$

$$\chi_j^{corr} = 0.0005 \times \chi_j + 0.0005 \times \chi_{j-1} \quad (3)$$

The simple Finite Impulse Response (FIR) low-pass filtering scheme of equation 3 ameliorates the effect of fast transients in the correction factor which could lead to unrealistic and flagrant discontinuities in the time array.

3. SOFTWARE ARCHITECTURE

The software structure of the EFCC controller application is founded on a framework developed within the JET Plasma Operations Group and reflects more than 15 years experience in plasma control and real-time applications. MARTe [4], the Multi-threaded Application Real-Time executor, is a multi-platform framework for rapid development and deployment of highly flexible, modular and easily maintainable real-time applications. It is also becoming widely adopted by different fusion related experiment devices such as COMPASS, ISTTOK and FTU, [5]. This framework is built upon the BaseLib2 C++ library which implements a real-time oriented set of layered functionality transparent to developers working in the Vx-Works, Linux, Linux/RTAI, Solaris and Windows operating system environments. In the particular case of this MARTe-based real-time application, VxWorks is the host operating system. MARTe provides not only the general infrastructure common to the vast majority of real-time control applications but also the set of communication, concurrency and debugging/introspection tools that enable the developer to focus almost exclusively on the specific problem to be solved. Ideally, and assuming the required hardware components are supported, the developer is only required to write the pieces of software dealing with the logic/algorithmic aspects specific to the control application itself. These software modules are called Generic Application Modules (GAMs) and are no more than the components that get executed in a top priority context within MARTe's real-time thread. This clear separation of generic and application specific functionality is enforced in MARTe's API which also imposes strict boundaries between hardware/synchronization (drivers), and algorithmic (application specific) software components.

A global overview of the controller applications' software architecture is given in figure 2. As a general outline, the user configures current reference waveforms using the Level-1 interface and loads the configuration into the controller application. The controller application is driven by an internal state machine which, in turn, is driven by JET's global state machine. MARTe acknowledges the state change request from the Supervisor software, updates its' internal state and dynamically sets the real-time thread to cycle through the appropriate set of GAMs. The philosophy behind GAMs is that they are self contained modular pieces of software obeying a specific programming interface and that they can only communicate with each other by reading and writing signals through an entity called Dynamic Data Buffer (DDB) which is no more than an enhanced, shared and managed data buffer. Interaction with external hardware components is performed at two levels. Low-level hardware support is provided as usual by manufacturers (or by developers based on manufacturers' supplied APIs) but there also exists an additional higher-level software layer obeying a specific programming interface which permits the usual i/o functionality to be performed in a hardware agnostic and standardized way. In this particular application, the entity called Driver Pool contains both the low-level and high level driver implementations that enable the usage of the same exact code (configured differently) for the Synchronisation, TimeCorrection, MPV922 Input and MPV956 Input GAMs as well as for the MPV922 Output and MPV956 Output GAMs thus, enabling seamless hardware input and output. Finally, there is the External Time Triggering Service (ETTS) which is responsible for the unblocking of the real-time thread, hence, the start of every control cycle at multiples of the configured cycle period. So, in every control cycle the GAMs illustrated in Figure 2 get called sequentially, each with its own functionality:

- Synchronisation GAM - gets unblocked by the ETTS on every multiple of 200μs given by the PowerPC oscillator;
- TimeCorrection GAM - reads in the corrected time information calculated within the VPLS driver;
- MPV922 Input GAM - reads the input from the digital board (currently not being used);
- MPV956 Input GAM - reads the analog inputs of measured EFCC currents and VCVSs output voltages;

- Waveform Generator GAM - generates the current reference waveform signals;
- PID GAM - calculates the voltage requests to be sent to the VCVSs based on the analog inputs;
- MPV922 Output GAM - sends a \heart-beat” digital signal to the plant in order to validate the analog voltage requests;
- MPV956 Output GAM - sends the analog voltage requests, calculated previously by the PID GAM, to the VCVSs;
- Data Collection GAM - stores signals for posterior placement in permanent storage following JET’s General Acquisition Program (GAP) requests;
- Web Statistic GAM - provides online, http-based, real-time monitoring of signals.

During the experiment, http clients can be used to monitor the application status and signal/variable values in real-time without affecting the application’s cycle time.

After the experiment, GAP requests the system’s raw data for permanent storage purposes following which the controller application is then ready and awaiting the next experiment.

A new Level-1 interface has been developed mainly to accommodate the Waveform Generator GAM used in the controller application. This interface allows the user to select multiple controller time windows and design the current reference waveforms allowing the exploitation of nearly all the functionality provided by the Waveform Generator GAM. In particular the concept of nested waveforms where a single waveform can contain attributes (offset, amplitude and frequency) which are also waveforms. This feature provides an enormous flexibility in the design of the experiments allowing for a vast exploitation of the system’s operational space.

4. PRELIMINARY RESULTS AND A NEW CONTROLLER SCHEME

An example preliminary result of the operation of this system is presented in figure 3 showing successful DC operation at the maximum achievable current.

It has been observed during JET operations that there is a decrease in the performance of this simple PID controller as the frequency of the current reference waveform increases. Furthermore, it is inevitable that inherent plant non-linearities such as component saturations and, in particular, the amplifier’s switching of the thyristor bridge restricts the performance of the (linear) PID controller to a limited operational space. This has motivated the design and development of a new non-linear and adaptive controller scheme with the clear aim of improving the system’s overall bandwidth.

The new controller, see figure 4, is based on the idea of shifting the current reference in time (Anticipation block) in order to compensate for circuit delays and the dynamics of the VCVS. The Inverse Model block calculates the inverse dynamics of the system thus supplying the feed forward component of the control voltage. Also, the Direct Model block is used in order to calculate the new reference for the PID which takes into account the anticipation mechanism. The anticipation mechanism is, in turn, driven by two dierent loops: the internal one, which attempts to synchronize the original reference with the newly calculated one (i.e. the one modified by the plant dynamics), and the outer one, which does the same with the new reference and the measured coil current.

The new controller algorithm has been developed and tested in Matlab®'s Simulink environment and simulation results are presented in figure 5. This figure shows a comparison between the experimentally achieved EFCC current and the predicted one by simulating the new controller algorithm for JET Pulse No: 79777. Furthermore, as a validation cross-check of the plant model used in the new controller algorithm, the simple PID behavior of the present controller has also been simulated revealing good agreement with the experimentally obtained current, thus, providing a clear indication of the accuracy of the model. The current reference used in this pulse is a 40Hz sinusoidal waveform and it can be seen that the simulation with the new controller scheme predicts an overall system bandwidth increase once it is implemented in the online system.

CONCLUSIONS

The new real-time controller application for the EFCCs has been commissioned and routinely used during the last JET campaign. Its graphical configuration interface provides a very efficient, user-friendly and intuitive facility for the regular user to configure the system and explore it in physics experiments. The flexibility and the facilities provided by the MARTe software framework were crucial tools not only in the development, deployment and commissioning activities but also envisaging the system's maintainability. The system has proven to perform well during JET operations in the case of DC or low frequency (≈10Hz) AC operation but clearly struggles in higher frequency cases nevertheless within the VCVS's specified bandwidth. The new controller introduced in the previous section is expected to increase the system's global bandwidth by a factor of Section 1 4, with its adaptive non-linear feed forward scheme, and is planned to be used in future JET operations.

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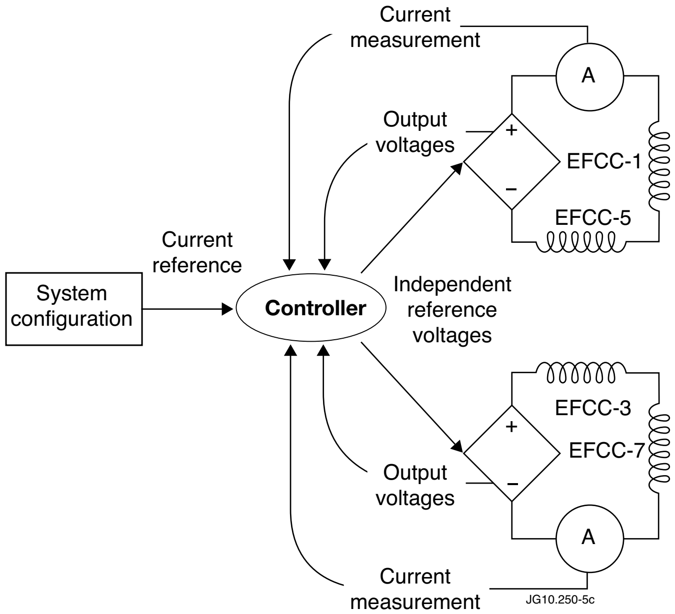

Figure 1: Scheme for creating the n = 1 magnetic configuration

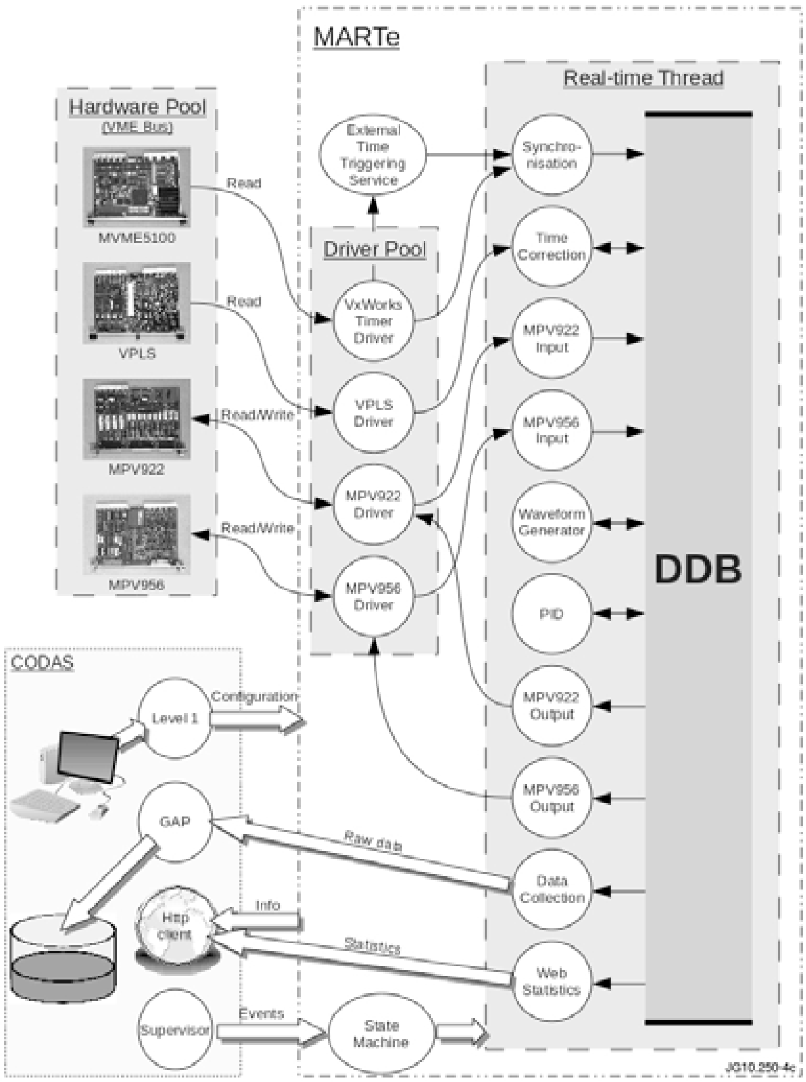

Figure 2: Software data flow diagram

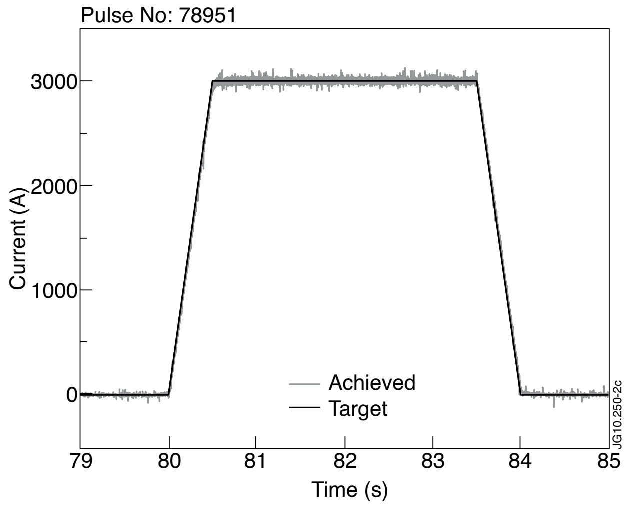

Figure 3: Results for Pulse No: 78951 - DC operation

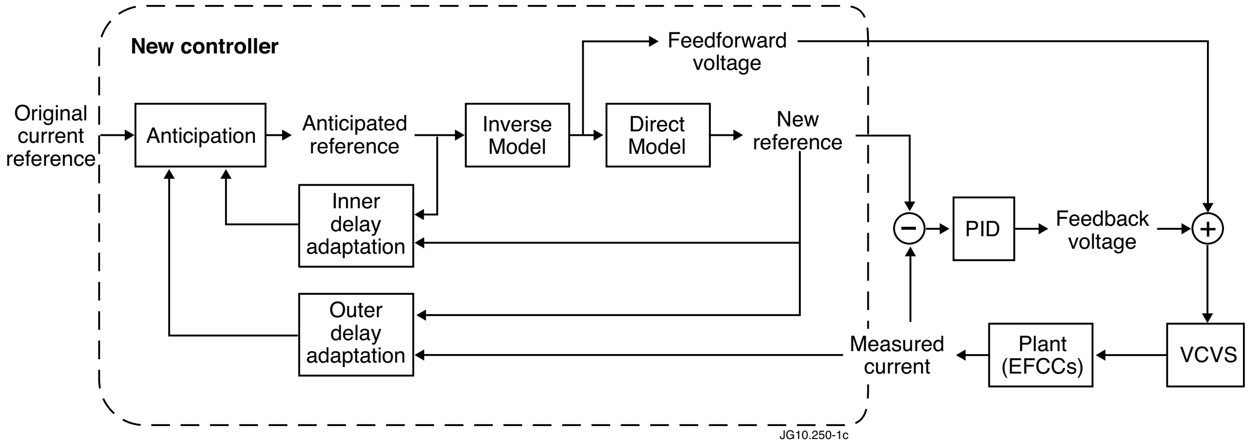

Figure 4: New controller diagram

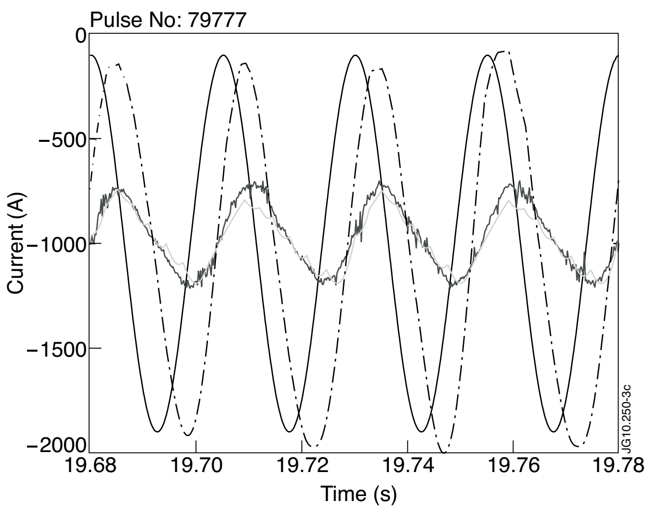

Figure 5: Comparison of simulated and experimental results - solid black line represents the reference waveform, dashed black line represents the simulated current obtained with the new controller, dark gray line represents the current experimentally obtained with the present PID controller and the light gray line represents the simulated current obtained with the present PID controller using the "plant model".