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Reconfigurable ATCA Hardware for Plasma Control and Data Acquisition

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ABSTRACT.
The IST/EURATOM Association is developing a new generation of control and data acquisition hardware for fusion experiments based on the ATCA architecture. This emerging open standard offers a significantly higher data throughput over a reliable High Availability (HA) mechanical and electrical platform. One of this ATCA boards has 32 galvanic isolated ADC channels (18 bit) each mounted on a swappable plug-in card, 8 DAC channels (16 bit), 8 digital I/O channels and embeds a high performance XILINX Virtex 4 family Field Programmable Gate Array (FPGA). The specific modular and configurable hardware design enables adaptable utilization of the board in dissimilar applications. The first configuration, specially developed for tokamak plasma Vertical Stabilization, consists of a Multiple-Input-Multiple-Output (MIMO) controller that is capable of feedback loops faster than 1 ms using a multitude of input signals fed from different boards communicating through the Aurora™ point-to-point protocol. Massive parallel algorithms can be implemented inside the FPGA either with programmed digital logic, using a HDL hardware description language, or inside included silicon PowerPC™ running a full fledged real-time operating system. The second board configuration is dedicated for transient recording of the entire 32 channels at 2 MSamples/s to the built-in 512 MB DDR2 memory. Signal data retrieval is accelerated by a DMA-driven PCI Express™ x1 Interface to the ATCA system controller providing an overall throughput in excess of 100MB/s. This paper illustrates these developments and discusses possible configurations for foreseen applications.

1. INTRODUCTION

Aiming to address the forthcoming challenges and the needs raised by the next generation of large scale physics experiments and in particular future Fusion devices like ITER, IST/EURATOM Association is developing a new generation of control and data acquisition hardware, based on the Advanced Telecommunications Computing Architecture (ATCA) architecture. This emerging open standard (PICMG 3.x) [1] is the largest specification effort made by PCI Industrial Computer Manufacturers Group and involving more than 100 companies mainly from the telecommunications industry and offers high throughput and High Availability (HA) and improved Reliability, Availability and Serviceability (RAS). The high throughput of the ATCA arises from its backplane architecture based on point-to-point protocol agnostic connections enabling high performance boards to communicate to each other over serial multi-Gbit/sec links, which is mandatory for the new generation CODAC (Control, Data Acquisition and Communications) systems that will implement Multi Input Multi-Output (MIMO) control schemes using thousands of input channels at a relatively low cost.

The ATCA High Availability (HA) and superior RAS capabilities derived from the shelf management system based on Intelligent Platform Management Interface (IPMI) [2], redundant power supplies and rugged mechanical specifications are particularly adequate for ITER [3] and other large-scale experiments requiring robust, fault tolerant, reliable, maintainable and secure CODAC capable of operating continuously over several months.

The ATCA platform is already being tested in tokamaks like JET, COMPASS, ISTTOK and other physics experiments as DESY or ATLAS at CERN.

Another important issue for modular architectures is the exploitation of the on-board reconfiguration options given by the Field Programmable Gate Array (FPGA) technology, which permits to adapt the same proven hardware platform on different specific applications.

Initially driven by some JET specific control and data acquisition upgrade projects like the Gamma ray cameras diagnostic [4] and plasma Vertical Stabilization (JET-VS) [5], but also envisaging for a much broader range of applications, IST/EURATOM Association developed a set of Control and Data acquisition ATCA hardware modules. One example is the high speed analog to digital converting and processing TRP module featuring 8 channels with 13 bit resolution, sampling at 25 MHz, 4GByte of local memory (SODIMM DDR2 DRAM) and two FPGAs able to perform complex trigger managing modes and allowing real time analyses (pulse height analyzer and pile-up discrimination), minimizing data storage and transfer issues [6]. The second inhouse development is a MIMO analog to digital module (32 galvanic isolated input plus 8 output channels) with control and processing capabilities, which represents a fine example where the modular a reconfigurable characteristics allow a wider range of applications. This paper will describe in detail this last module applied to very distinct applications, one for the JET-VS control system and the other for the COMPASS tokamak data acquisition system.

2. THE ATCA MIMO-ISOL HARDWARE

2.1 MODULE ARCHITECTURE

The ATCA hardware module developed at IST [7] for control and data acquisition purposes comprises i) a main board, ii) a carrier board for input channel sub-modules, and a Rear Transition Module (RTM) (Fig 1). The main board comprise the FPGA device Xilinx® Virtex™ 4 (XC4VFX60/100), the associated CompactFlash (CF) memory for the configuration firmware, the SODIMM DDR2 data memory (512MB), clock/trigger circuiting, the DC-DC converters, the two ATCA backplane connectors (power and data communication) and an edge connector for the RTM board. All the supply voltages are generated from the standard ATCA -48V power connector. The second connector routes the PCI Express (PCIe) interconnection to the crate controller and all the point-point links to every other modules on the same crate over the full mesh fabric.

The module generic architecture, depicted in Fig.2, clearly illustrates one crucial aspect of the overall design: all the different functional blocks connect directly to the central reconfigurable FPGA through non shared data paths. With this approach the only constrains to the developer are the internal resources provided by the specific FPGA. It is possible to implement virtually any type of internal configuration, signal routing or data processing.

2.2 ADC SUB-MODULES

The carrier board, seen of the left side of Fig.1, holds the 32ADC 1kV isolated input channel plugin

modules. Each one of these individual submodules is capable of converting a differential analog signal, with a dynamic range up to +−32V, at 2Msamples/sec with 18 bit resolution. The analog front end includes a 3rd-order passive anti-aliasing filter. The galvanic isolation barrier, using magnetic couplers is located in the downstream digital signal serial path. These plug-in modules can be replaced at anytime with different design and functionalities, providing, for example, extra input signal amplification or other type of analog processing (e.g. analog integrators). All the external input signals connect through four D-37 type connectors mounted on the front side-panel.

2.2 REAR TRANSITION MODULE

The RTM board is optionally installed on the rear part of the ATCA crate and contains the DACs for the 8 analog output channels (+-10V), 8 digital I/O channels (EIA-485) and a multi-gigabit/s optical SFP connector. External timing and clock signal are typically connected to the RTM of one hardware module, designated as the Master. After a PLL type synchronization they are distributed over the ATCA backplane shared lines so that every module in the same crate receives exactly the same signal. Only one specific module can be assigned as a Master on the same crate. This is automatically established by the firmware by reading the ATCA hardware slot address and matching a pre-programmed value.

3. JET-VS CONTROLLER HARDWARE CONFIGURATION

3.1. CONTROLLER SYSTEM ARCHITECTURE

The JET Vertical Stabilization upgrade project consists in a complete re-design of the control system for the vertical instability appearing in elongated plasmas with the expected ability to recover from large ELM perturbations (> 1MJ). This system monitors a total 192 signals (128 magnetic plus auxiliary) and actuates on a set of the PF coils. The requirements established by the project proposal included new targets for the loop delay (down to 10μs), a digital link between the controller and the actuator and a much higher processing power needed for a redesigned decoupler-controller MIMO type algorithm.

The present JET configuration uses a single ATCA crate with a custom developed main controller module and six ATCA-MIMO-ISOL hardware modules. The crate controller-processor blade is based in a low cost ATX form motherboard equipped with a Intel quad-core x86 CPU mounted on a locally developed ATCA-form PCIe switch board. All the six main modules can be interconnected by Aurora™ 2.5Gb/s low-latency links via the ATCA full-mesh backplane, allowing all channel data to be available, in the control cycle, on each FPGA running a future distributed control algorithm expected to attain a 10μs loop-cycle. However this powerful network is not yet implemented and the modules presently connect to the main controller in a star topology over the ATCA backplane by means of PCIe x1 connections. As a result the system currently attains a control loopcycle time of 50μs with a jitter inferior to 1μs. Consequently the original 2MSample/s channel data stream is to be decimated by a factor 1:100.

3.2. FIRMWARE ARCHITECTURE

In this firmware design the main goal was to create a continuous stream data acquisition with lowest possible latency from the ADC modules to the central CPU where the control algorithms are computed on a Real-Time OS. The present FPGA configuration for the VS project is depicted in Fig.3. Inside the FPGA, data from the ADC is first deserialized then goes through a 100 tap FIR digital anti-aliasing filter and finally to the a 20kSample/s decimator. All this data processing runs evidently in parallel. The 32x1 MUX then feeds a DMA engine associated to the PCIe endpoint logic, which creates periodically data packets containing all 32 simultaneous samples and transmits them as "posted" PCIe Transaction Layer Packet (TLP) to the CPU board main memory. Furthermore to minimize latency, after each DMA transfer, fresh data in the main memory is signalled not by CPU interrupts as usual but instead with a much faster software polling routine. In addition, the firmware includes a set of memory-mapped registers that can be accessed through the Programmed Input Output (PIO) operations from the PCIe to control the internal operation of the board, read status, and also to drive the DAC outputs. Timing and synchronization of modules is provided by shared lines on the ATCA backplane driven by the master module.

3.3. SOFTWARE ARCHITECTURE

To guarantee real-time execution of the control codes all the software for the VS control system is based in the Multi-threaded Application Real-Time executor (MARTe) [8], developed at JET. MARTe is a real-time, modular and layered C++ framework that includes among other functionalities a highly creation configuration, built-in object introspection and garbage collection. The user control algorithms are implemented inside well-defined blocks of software, named Generic Application Modules (GAM). All the GAMs are executed by the real-time scheduler of the Real Time Application Interface (RTAI)/Linux operating system exploiting the new x86 multi-core processors technology.

4. COMPASS DATA ACQUISITION HARDWARE CONFIGURATION

The COMPASS tokamak was recommissioned recently in IPP-CZ Prague [9] and is starting now its operation with a totally redesigned ATCA-based CODAC (Fig. 4) [10]. The installed plasma control system is a similar though reduced version of the JET VS controller, using the same software framework tools and drivers but only one single previously described ATCA-MIMO-ISOL module and firmware running customized GAMs for COMPASS plasma control [11].

4.1. COMPASS REDESIGNED FIRMWARE

Data acquisition for the plasma diagnostics is based on thirteen other ATCA-MIMO-ISOL similar modules installed on two CODAC ATCA crate nodes each one with an x86 quad-core based controller blade running the RTAI Linux OS. However, the module's main FPGA uses a completely redesigned firmware that changes its functionality. The main objective is the acquisition of all the diagnostic signals at the ADC full specified resolution of 2MSamples/s at 18-bit resolution. For that reason, it

is not possible to stream the this large amount data from the 32 channels times 13 modules to the main CPU board through the PCIe x1 connections in real-time. The solution is to use the 512MB DRAM memory to store channel data for each plasma discharge and the module behaves as a transient recorder, collecting up to 2 seconds of continuous data for every channel. The new firmware for the COMPASS ATCA-MIMO-ISOL module was developed and implemented from scratch in Verilog language. The project compilation was carried using XILINX ISE 10.1 software tools.

Figure 5 depicts the new internal FPGA configuration. In this memory-based schematic, once the trigger is received, channel data from the ADC sub-modules start filling the DRAM memory into 32 equally sized regions (16MB). On acquisition completion, the PCIe control logic interrupts the crate controller's CPU, which can afterwards initiate the data collection. Data transfer is accelerated using a series of interrupt-based DMA operations programmed by the CPU, each sending 4096 bytes to a Linux kernel's memory buffer. A total data throughput of 120MB /s was measured between the modules and the crate controller using a test user mode application.

4.2. TIMING AND TRIGGER

The trigger and timing on COMPASS will depend on the Aurora™ link-layer protocol based Event and Timing Network (ETN) developed jointly for COMPASS and ISTTOK tokamaks over pointto-point links. The firmware provides a connection to this network by an Aurora™ 2.5 Gb/s optical link. A central Event & Trigger PCI [12] board installed on a NTP-synchronized PC and connected to the ETN periodically broadcasts an absolute time with a 8 ns resolution using high priority Aurora protocol's User Flow Control (UFC) 64 bit messages. The master acquisition module on each the crate receive this absolute time, re-syncs its internal time counter, and can also recover the 125Mhz synchronous clock from the optical link. From this recovered clock the firmware generates a 2MHz acquisition clock that is distributed to other slave modules on the same crate over the backplane. All the modules trigger simultaneously on external events received by the master or in a pre-programmed absolute time schedule.

4.3. SOFTWARE ARCHITECTURE

The software support for these modules is provided by the FireSignal (FS) [13] distributed control and data acquisition framework developed at IST. A new specific interface component, named Hardware Node (HN), was developed in C++ language, using the Common Object Request Broker Architecture (CORBA) protocol for network communications and eXtensible Markup Language (XML) files for hardware self-description. With this component the FireSignal system generates a customized GUI, which allows the machine operator to configure the acquisition and to follow the results. The FS system can also pre-program a set of trigger events on the HNs connected in the system. On this specific HN they can be: i) an immediate soft trigger, ii) arming for an external hardware trigger, and iii) an absolute time trigger. When this last trigger type is chosen the module starts acquisition when its internal time counter attains a pre-programmed value. After plasma

discharge completion, the HN application is responsible to fetch sample data from all the acquisition modules in the system and to send it to FireSignal server to be stored on the central database. The module device driver for the Linux OS version 2.6.20 was written in C language.

4.4. FUTURE FIRMWARE DEVELOPMENTS

Plans to improve the ATCA-MIMO-ISOL firmware functionalities include support for larger capacity DRAM SODIMM, multi-rate data acquisition, signal online digital filtering, event detection algorithms generating real-time messages for other CODAC nodes over the ETN links and the implementation of the Power PC hardware core included in Xilinx® Virtex™ 4 devices, running a Linux OS, for enhanced data and event processing.

CONCLUSION

The ATCA standard presents a promising technology platform to develop complex, reliable upgradeable and scalable control and data acquisition systems for physics experiments and fusion devices in particular and is already appearing of several machines like JET, COMPASS or ISTTOK. This paper demonstrates the use of this technology allied to modular hardware design and the reconfigurable configuration feature of FPGA devices enabling the re-use of hardware components on two distinctive applications. The presented distributed parallel type data processing, point-to-point multi-Gbit/s serial links for timing, event and data communication and advanced software frameworks symbolize some of the essential building blocks for next generation CODAC systems.

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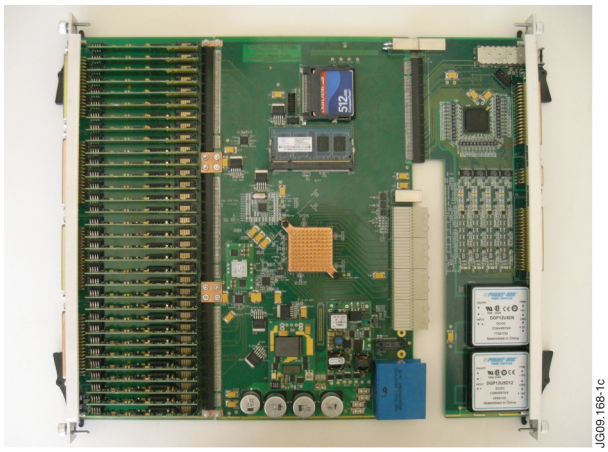

Figure 1: ATCA-MIMO-ISOL module top view (including the ADC modules carrier board, main controller and Rear Transition Module board).

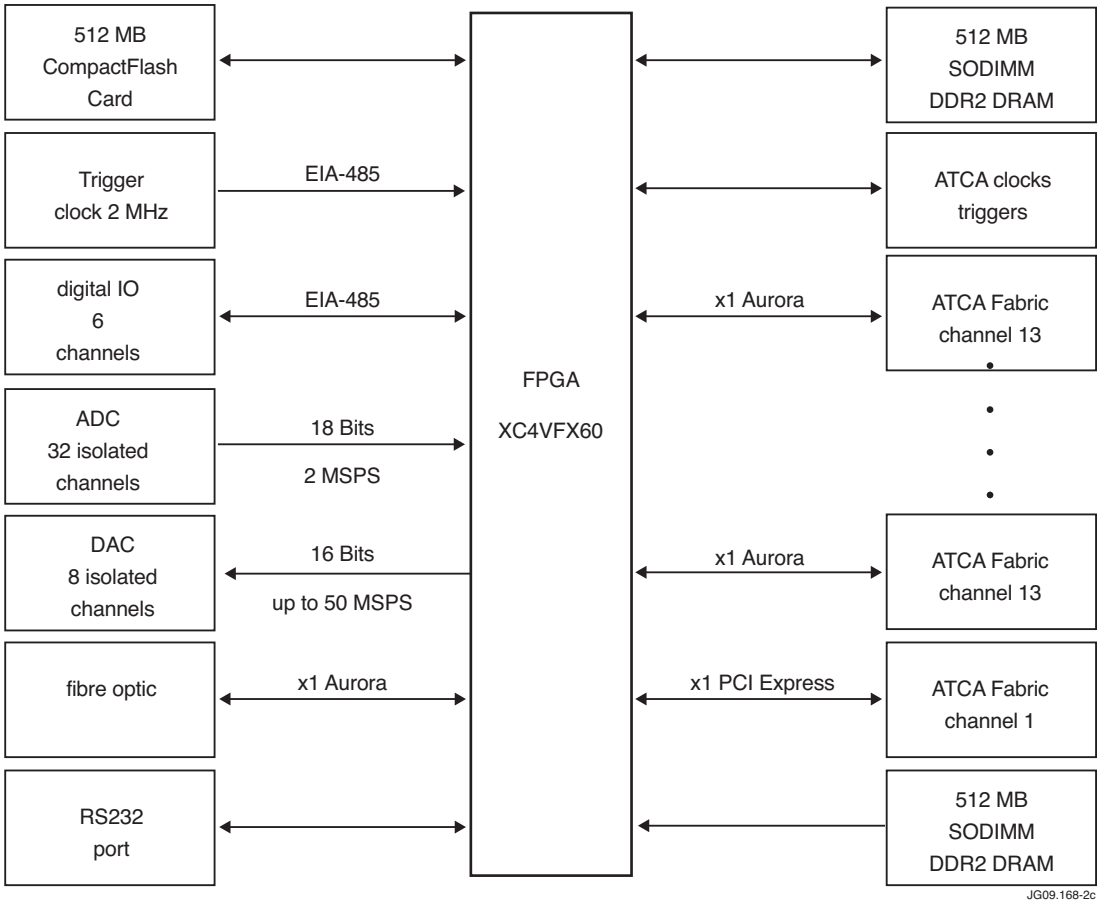

Figure 2: ATCA-MIMO-ISOL module hardware block architecture.

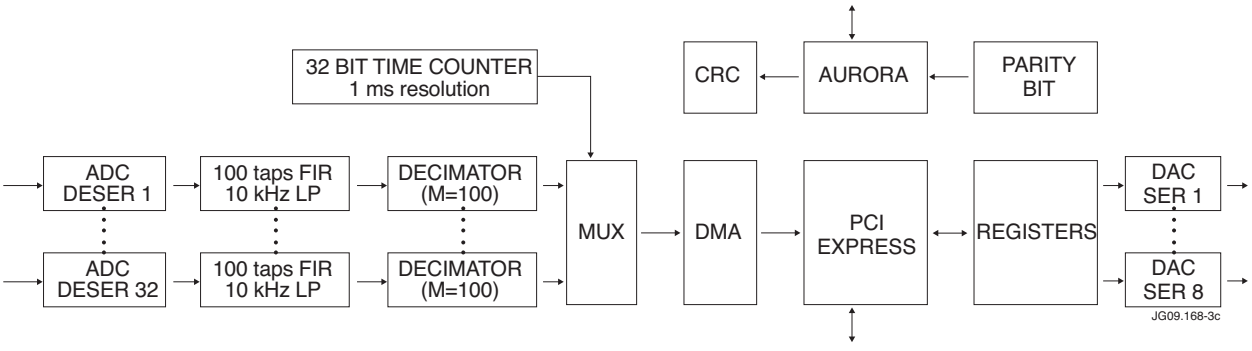

Figure 3: VS Controller Hardware module firmware block diagram.

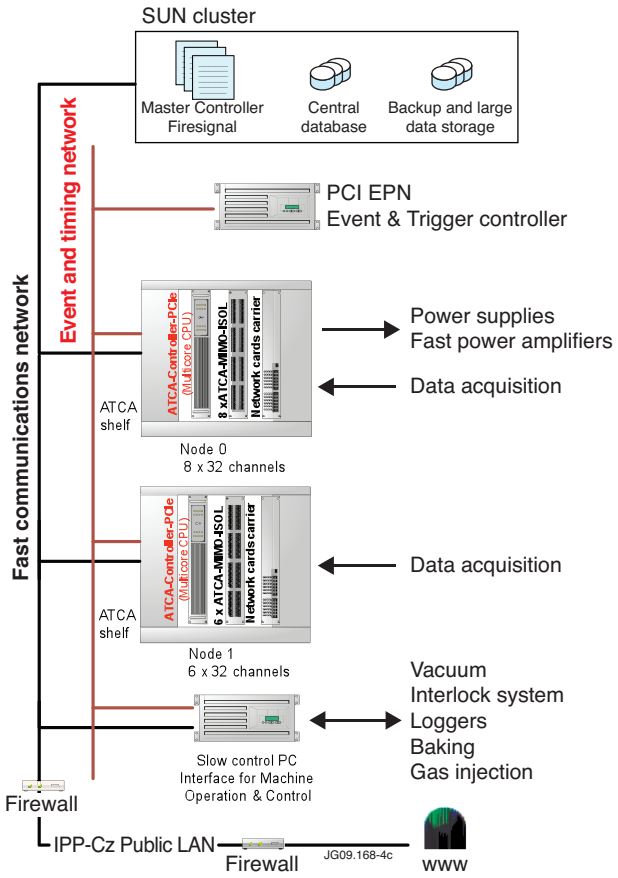

Figure 4: Schematic of the redesigned COMPASS tokamak control and data acquisition system.

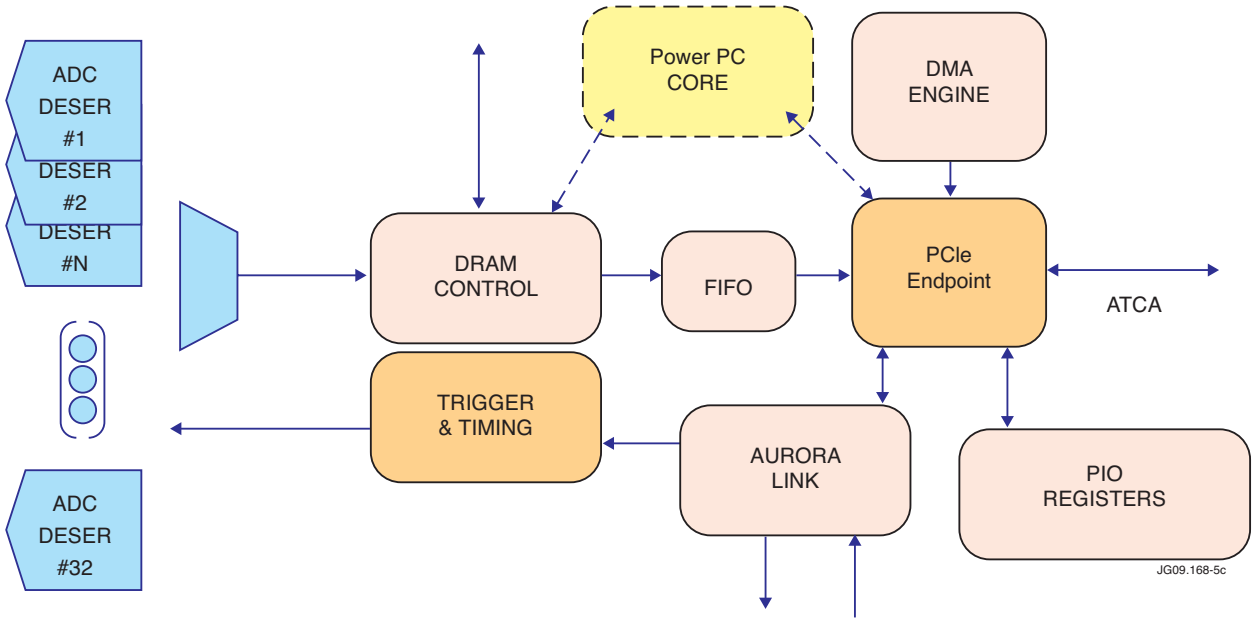

Figure 5: COMPASS data acquisition firmware block diagram.