

A.M. Fernandes, R.C. Pereira, J. Sousa, A. Neto, P. Carvalho, A.J.N. Batista,
B.B. Carvalho, C.A.F. Varandas, M. Tardocchi, G. Gorini
and JET EFDA contributors

Parallel Processing Method for High Speed Real Time Digital Pulse Processing for Gamma-Ray Spectroscopy

“This document is intended for publication in the open literature. It is made available on the understanding that it may not be further circulated and extracts or references may not be published prior to publication of the original when applicable, or without the consent of the Publications Officer, EFDA, Culham Science Centre, Abingdon, Oxon, OX14 3DB, UK.”

“Enquiries about Copyright and reproduction should be addressed to the Publications Officer, EFDA, Culham Science Centre, Abingdon, Oxon, OX14 3DB, UK.”

The contents of this preprint and all other JET EFDA Preprints and Conference Papers are available to view online free at www.iop.org/Jet. This site has full search facilities and e-mail alert options. The diagrams contained within the PDFs on this site are hyperlinked from the year 1996 onwards.

Parallel Processing Method for High Speed Real Time Digital Pulse Processing for Gamma-Ray Spectroscopy

A.M. Fernandes¹, R.C. Pereira¹, J. Sousa¹, A. Neto¹, P. Carvalho¹, A.J.N. Batista¹,
B.B. Carvalho¹, C.A.F. Varandas¹, M. Tardocchi², G. Gorini²
and JET EFDA contributors*

JET-EFDA, Culham Science Centre, OX14 3DB, Abingdon, UK

¹*Associação EURATOM/IST Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico,
1049-001 Lisboa, Portugal*

²*Università degli Studi di Milano-Bicocca Istituto di Fisica del Plasma,
EURATOM-ENEA-CNR Association, I-20125 Milan, Italy*

** See annex of F. Romanelli et al, "Overview of JET Results",
(Proc. 22nd IAEA Fusion Energy Conference, Geneva, Switzerland (2008)).*

Preprint of Paper to be submitted for publication in Proceedings of the
7th Technical Meeting on Control, Data Acquisition and Remote Participation for Fusion Research,
Aix-en-Provence, France.
(15th June 2009 - 19th June 2009)

ABSTRACT

A new data acquisition (DAQ) system was developed to fulfil the requirements of the Gamma-Ray Spectrometer (GRS) JET – EP2 (joint European Torus enhancement project 2), providing high-resolution spectroscopy at very high count rate (up to few MHz). The system is based on the Advanced Telecommunications Computing ArchitectureTM (ATCATM) and includes a Transient Record (TR) module with 8 channels of 14 bits resolution at 400 MSamples/s (MSPS) sampling rate, 4GB of local memory, and 2 field programmable gate array (FPGA) able to perform real time algorithms for data reduction and digital pulse processing.

Although at 400 MSPS only fast programmable devices such as FPGAs can be used either for data processing and data transfer, FPGA resources also present speed limitation at some specific tasks, leading to an unavoidable data lost when demanding algorithms are applied. To overcome this problem and foreseeing an increase of the algorithm complexity, a new digital parallel filter was developed, aiming to perform real time pulse processing in the FPGAs of the TR module at the presented sampling rate. The filter is based on the conventional digital time invariant trapezoidal shaper operating with parallelized data while performing Pulse Height Analysis (PHA) and Pile Up Rejection (PUR). The incoming sampled data is successively parallelized and fed into the processing algorithm block at one fourth of the sampling rate. The following data processing and data transfer is also performed at one fourth of the sampling rate.

The algorithm based on data parallelization technique was implemented and tested at JET facilities, where a spectrum was obtained. Attending to the observed results, the PHA algorithm will be improved by implementing the pulse pile up discrimination.

1. Introduction

The Gamma-Ray Spectrometer (GRS) is one of the methods used to study the fast particles behavior in tokamaks allowing a direct measurement of the rates at which the energy production reactions occurs [1]. The JET – EP2 program aims to excel some limitations as energy resolution signal background and time resolution, inherent to the existing GRS diagnostics [2, 3], and fully exploit the flux increase provided by future high power experiments at JET and ITER [2, 3]. One of the program tasks is the development of a new DAQ system capable to perform high-resolution spectroscopy at very high count rate.

The DAQ system is based on ATCATM [4] and includes a multi-core x86-based General Purpose Processor (GPP) composed by an Advanced Technology Extended (ATX) motherboard linked to a PCI Express (PCIe) switch through x16 PCIe lane [5] and a Transient Record (TR) module interconnected through x4 PCIe links. This DAQ system will be interfaced to the JET Control and Data Acquisition System (CODAS) through a FireSignal node [6].

The TR module comprises two blocks, each with 4 channels of 14-bit resolution at up to 400 MSamples/s (MSPS) sampling rate (ADS5474), 2GB Double Data Rate Synchronous Dynamic Random Access Memory (DDR2 SDRAM), and an FPGA from XilinxTM Virtex 4 family

(XC4VFX60-1152) [7].

The FPGAs act as the module core and are responsible for (i) Controlling analogue inputs calibration, clocks configuration and triggering modes; (ii) Interfacing local memory and gigabit communication through PCIe links; (iii) Managing local memory data storage and reading; and (iv) Data reduction/processing: Performing data reduction based on real time digital pulse processing.

Although at 400 MSPS only fast programmable devices such as FPGAs can be used for both data transfer and data processing, at such high sampling rate, also some FPGA resources have speed limitation when performing some specific tasks (e.g. 400MSPS are out of Virtex-4 first in first out memory's (FIFO) range [8]) leading to an unavoidable data loss. To overcome this limitation all acquired data is parallelized and sampled at one fourth of the sampling rate, as described in section 2. Moreover, this method also allows extending the algorithm complexity, and opens the possibility of interleaving channels to increase the sampling rate.

2. DATA PARALLELIZATION METHOD

The 14-bit of each free-running ADC channel are directly attached to the FPGA, where data goes through several real time buffering and processing stages before being transferred to local memory, as depicted in fig.1.

At the first stage (pre buffer block) the signal is applied to Input Dual Data Rate (IDDR) dedicated registers and converted into a 16-bit word. The second stage comprises a parallel buffer block, where a FIFO with independent I/O clocks builds a 64-bit word composed by four 16-bit parallel words, sampled at one fourth of the input clock (parallelized data). Data output shares three simultaneous paths. Depending on the selected operating mode, the correspondent output is stored at local memory and later retrieved through PCIe links. The three operating modes are: (i) Raw data – all acquired data is stored in local memory; (ii) Pulse data – only pulses, identified with a 64-bit time stamp header (pulse event time), are stored in local memory, leading to a significant reduction of irrelevant incoming data; (iii) Processed data – real time pulse processing algorithms are applied to perform PHA with PUR, returning a 48-bit time stamp plus 16 bit pulse energy (64-bit word) per detected pulse.

The first and second operating modes do not require fine changes when parallelized data is performed. The exception occurs when a complex trigger threshold algorithm for pulse detection in the second mode is applied (e.g. when averages are used).

The third block performs complex algorithms for parallel pulse processing which requires the careful selection of a frame, as described in the following section.

3. PARALLEL PULSE PROCESSING

The processed data operation block is one of the most desirable goals to be attained with the TR module. While in raw data mode at 400MSPS the 2GB memory will be filled up by one channel in 2.5 seconds, in the processed mode estimating 2Mevents/s it will take ~ 2 minutes to be filled up,

which is a significant increase in the number of useful stored data.

The developed parallel pulse processing algorithm implemented in the FPGA is based on the conventional time-invariant Digital Trapezoidal Shaper (DTS), well known from literature as a powerful technique in high resolution and high count rate pulse spectroscopy [9].

Considering the trapezoid as an Infinite Impulse Response filter (IIR), where the output always depends on previous inputs in a serial behavior, the novelty is the ability to perform pulse processing regarding parallel data as if it was in series.

As shown in fig.2, the developed parallel algorithm is composed by the DTS, the Edge Detector (ED) and the Energy Resolver (ER) modules, described in sections 3.1 to 3.3. Parallel input data ($v_n(t)$) should be assumed as a matrix of 4×16 (four 16-bit words).

3.1 DTS MODULE

DTS is the module that performs recursive parallel trapezoid filter applying the following equations, deduced from the conventional trapezoidal forms [10]:

$$d_n^{kl}(t) = v_n(t) - v_{n-x}(t-k) - v_n(t-l) + v_n(t-k-k) \quad (1)$$

$$p_n(t) = p_3(t-1) + \sum_{i=0}^n d_n^{kl}(t) \quad (2)$$

$$r_n(t) = p_n + M \times d_n^{kl}(t) \quad (3)$$

$$s_n(t) = s_3(t-1) + \sum_{i=0}^n r_i(t) \quad (4)$$

where $n = [0.3]$ represents each parallel data and t is the sampling period.

Equation (1) performs the first stage of the DTS module, composed by two delays-subtract units, in series: the Fine aDjuSt delay (FDS) and the Coarse aDjuSt delay (CDS). Data is delayed by user defined variables K and L , respectively, and subtracted to the present data. K delay variable, from FDS unit, ranges from 0 to 15 and is capable of subtracting data from different raw positions as unit steps are allowed ($x = [0.3]$). L delay variable, from CDS unit, ranges from 0 to 255 in steps of four (only subtractions between data at the same raw position are permitted).

The $d_n^{k,l}(t)$ outcome follows to the High Pass filter Deconvolver (HPD) composed by an accumulator $p_n(t)$ (eq.2) which result is summed to the signal adjustable pole-zero cancelation (parameter M calculated accordingly to the pulse decay time constant f) returning $r_n(t)$ (eq.3). When HPD is supplied with a sampled exponential pulse with f , it returns a step signal that can be used to calculate the pulse energy. The last ACCumulation (ACC) given by $s_n(t)$ (eq. 4) completes the trapezoid.

Since DTS is a linear time-invariant system, the units order is neutral, however to avoid an overflow due to the accumulations, the HPD is placed after de FDS and CDS units. As a result,

DTS converts each acquired exponential pulse into a symmetrical trapezoid with a rising (falling) edge length given by the minimum between K and L and a flat top length equal to the absolute value of the difference between K and L [10].

Due to accumulations and sums (to avoid overflow) all the HPD equations as well as present a 32-bit length.

3.2. ED MODULE

Simultaneously with the DTS unit, an Edge Detector (ED) triggers each time one of the four parallel data reaches the pre-defined threshold. The ED returns a four bit word, related to the data raw position and aligned with the trapezoid output ($s_n(t)$). In the presence of a trigger the corresponding ED bit goes high.

The trigger is calculated by the difference between the average values (1, 2 or 4) of successive samples. The average is used to provide a trigger less sensitive to gaps oscillation between acquired values [11]. According to the example depicted in figure 3, if a trigger event is present.

3.3. ER MODULE

The Energy Resolver (ER) is the last module of the processing block and receive and as inputs. When signals a trigger event, presents the trapezoidal shape of the detected pulse and the resolver starts to calculate the corresponding pulse energy that is determined by the difference between flat top values (E) and the estimated Baseline (B) of the trapezoids. The algorithm flowchart is depicted in fig.4.

When a trigger event occurs, the x variable is set to zero and is incremented at each fourth of the sampling clock frequency. If $k < x < l$, equations (5) and (6) are applied:

$$E = E + \sum_{i=0}^n s_i(x) \quad (5)$$

$$B = B + \sum_{i=0}^n s_i(x-l) \quad (6)$$

While x is smaller than $2L + K$ (well defined trapezoid), and if no other trigger events occur, the energy of this event (E_r) is calculated ($E_r = E - B$).

Note that although ER outcome isn't parallelized data, it is still sampled at one fourth of the input sampling rate. is converted to 16-bit word and signaled with the related 48-bit time stamp, returning a 64-bit word from the module.

4. RESULTS

The presented parallel pulse processing algorithm was implemented in the ATCA TR module and tested with pulses from a raw data base restored in a Tektronix Arbitrary waveform generator

(AWG420). Figure 5 depicts, as example, one of the acquired pulses from raw data operating mode and the corresponding trapezoidal output . For calibration purposes, the plot is possible in an extra operating mode, the calibration mode (not to be used during normal TR operation). It is also shown the gamma ray single energy plus noise distribution spectra obtained with the processed operating mode acquisition.

To evaluate the method efficiency, the same pulses were applied to an offline not parallelized algorithm running in a standard PC. Comparing both spectra it was concluded that the conventional time-invariant digital trapezoidal shaper validity is ensured using the parallelized method. The parallelized algorithm is also being tested at JET facilities.

CONCLUSIONS

The processing operating mode is one of the tasks to be attained with the TR module due to the significant increase in the number of useful stored data, when compared with the raw data operating mode.

In order to prevent data losses due to speed limitations in some FPGA resources at high sampling rate, foreseen an increase in algorithm complexity and provide interleaved architectures between channels, the parallelized processing method, based on classical trapezoidal filter, was developed. The developed parallelization method may also be used as interface to other processing algorithms (e.g. less pulse shape dependence than the trapezoidal filter), subjected to the FPGA resources availability.

Attending to the results obtained with pulses restored in AWG420 it was concluded that the classical filter validity is ensured using the parallelized method.

To overcome some limitations inherent to the classical trapezoidal shaper next steps are being considered for baseline restoration, since the performance of an IIR filter drops if the signal baseline is not stable [12], and for the pulse pile up discriminator capability.

ACKNOWLEDGEMENTS

This work has been sponsored by the Contract of Association between European Atomic Energy Community and Instituto Superior Técnico (IST) and by the Contract of Associated Laboratory between Fundação para a Ciência e Tecnologia (FCT) and IST. The content of publication is the sole responsibility of the authors and it does not necessarily represent the views of the Commission of the European Union or FCT or their services.

REFERENCES

- [1]. V.G. Kiptily, et al., \geq ray diagnostics of energetic ions in JET, Nuclear Fusion **42** (2002) 999–1007.
- [2]. M. Tardocchi et al, Gamma ray spectroscopy at high energy and high time resolution at JET, Rev. of Scientific Instruments, **79** (2008) 10E524.

- [3]. JET-EP2 - Project Plan: “Gamma-ray spectrometry-GRS”, 2006, JET internal document.
- [4]. AdvancedTCA®, PICMG® 3.0 Revision 2.0, AdvancedTCA® Base Specification, March 18, 2005.
- [5]. A.J.N. Batista, J. Sousa, and C.A.F. Varandas, ATCA digital controller hardware for vertical stabilization of plasmas in tokamaks, *Review of Scientific Instruments*, **77**, no. 10 (2006).
- [6]. A. Neto, J. Sousa, B. Carvalho, H. Fernandes, R. C. Pereira, A. M. Fernandes, C. A. F. Varandas, G. Gorini, M. Tardocchi, D. Gin, A. Shevelev and K. Kneupner, “The control and data acquisition software for the gamma-ray spectroscopy ATCA sub-systems of the JET-EP2 enhancements” *Fusion Engineering and Design* **83** (2008) 346-349.
- [7]. R.C. Pereira J.Sousa, A.M. Fernandes, F. Patrício, B. Carvalho, A.Neto, C.A.F. Varandas, G. Gorini, M. Tardocchi, D.Gin, A. Shevelev, ATCA data acquisition system for gamma ray spectrometry, *Journal of Fusion Engineering and Design* **83** (2008) 341–345.
- [8]. FIFO Generator v4.2 User Guide, UG175 Oct 10 (2007) <http://www.xilinx.com/>.
- [9]. V.T. Jordanov, Glenn F. Knoll, Digital synthesis of pulse shapes in real time for high resolution radiation spectroscopy, *Nuclear Instrum. Meth. Phys. Res. A* **345** (1994) 337-345.
- [10]. V.T. Jordanov et al, Digital techniques for real-time pulse shaping in radiation measurements, *Nuclear Instrum. Meth. Phys. Res. A* **353** (1994) 261–264.
- [11]. A. Combo R. Pereira, J. Sousa, N. Cruz, P. Carvalho, C. A. F. Varandas, S. Conroy, J. Källne and M. Weiszflog, A PCI transient recorder module for the JET magnetic proton recoil neutron spectrometer, *Fusion Engineering and Design* **71** (2004) 151–157.
- [12]. Wuyun Xiao, Yixiang Wei, Xianyun Ai and Qi Ao, System simulation of digital pulse spectrometer, *Nuclear Instrum. Meth. Phys. Res. A* **555** (2005) 231–235.

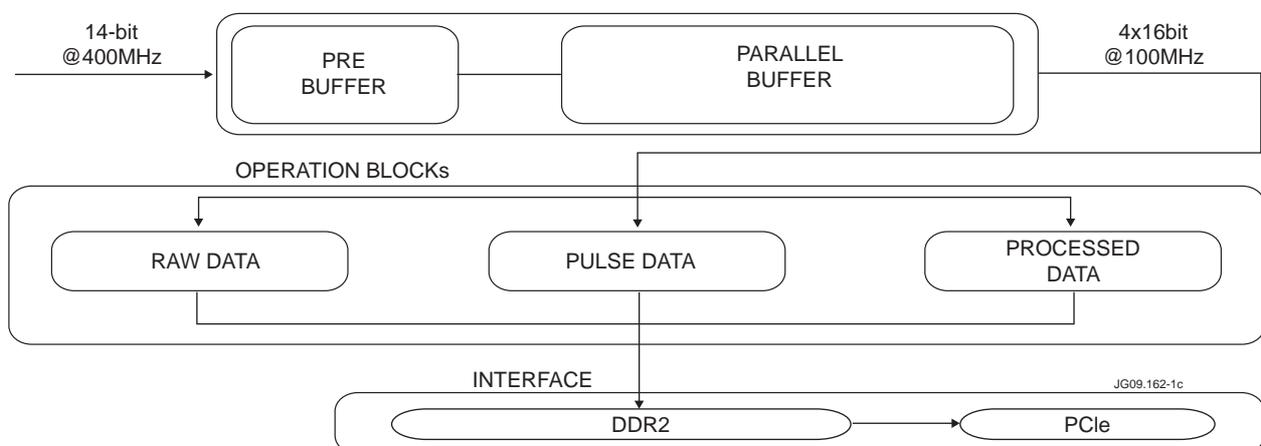


Figure 1: FPGA stages diagram. The input 14-bit@400MHz acquired data is buffered and parallelized into a 4x16-bit@100MHz word and then sent to the three operating blocks. The chosen operation mode is stored at local memory and later retrieved through PCIe links.

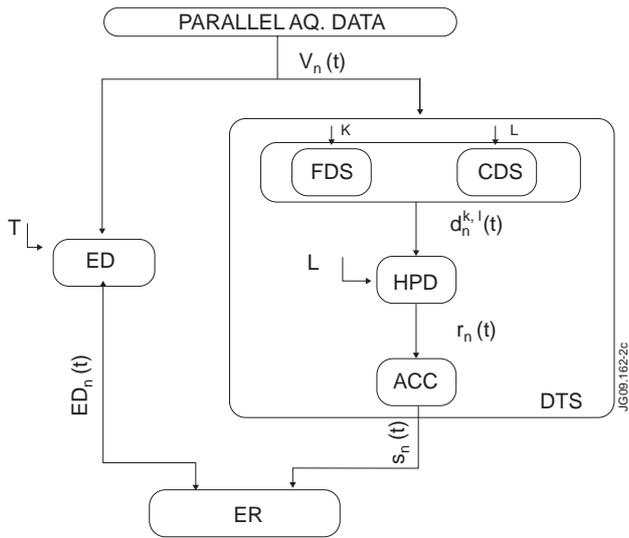


Figure 2: Parallel pulse processing diagram. The input parallelized data $v_n(t)$ goes to the DTS module to apply the trapezoidal filter and to the ED module to detect trigger events. The returning result follows to the ER module to perform PHA with PUR.

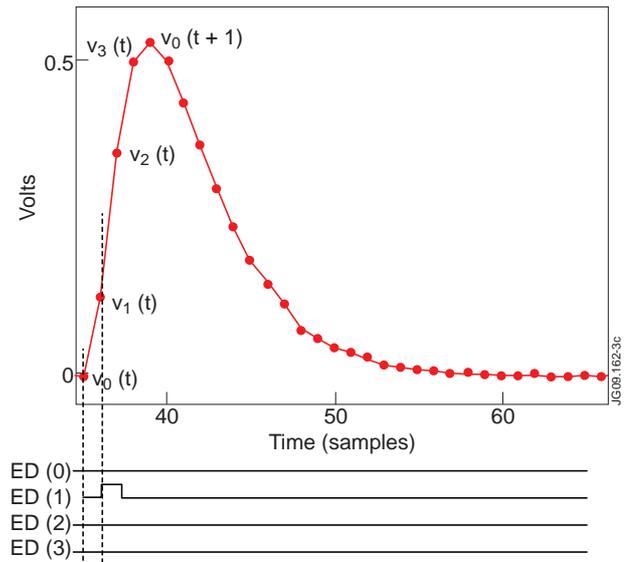


Figure 3: Trigger edge detection scheme. When one of the four parallel data reaches the pre-defined threshold, meaning that a trigger event is present.

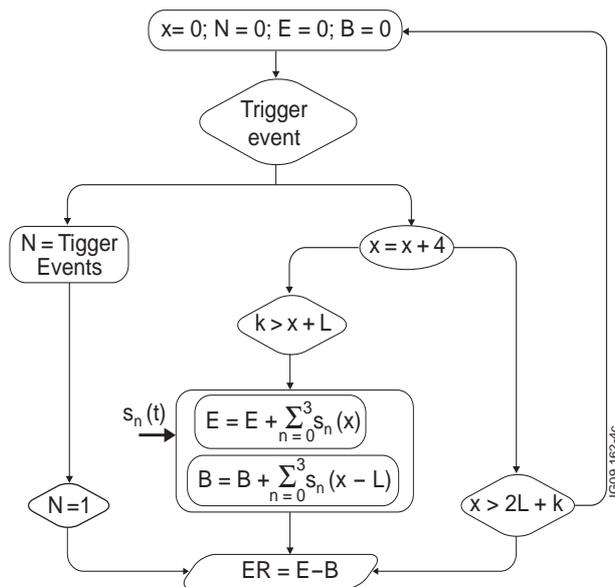


Figure 4: ER Flowchart. When a trigger event occurs the ER starts to calculate the corresponding pulse energy, which value is considered if no other trigger events occur during this pulse.

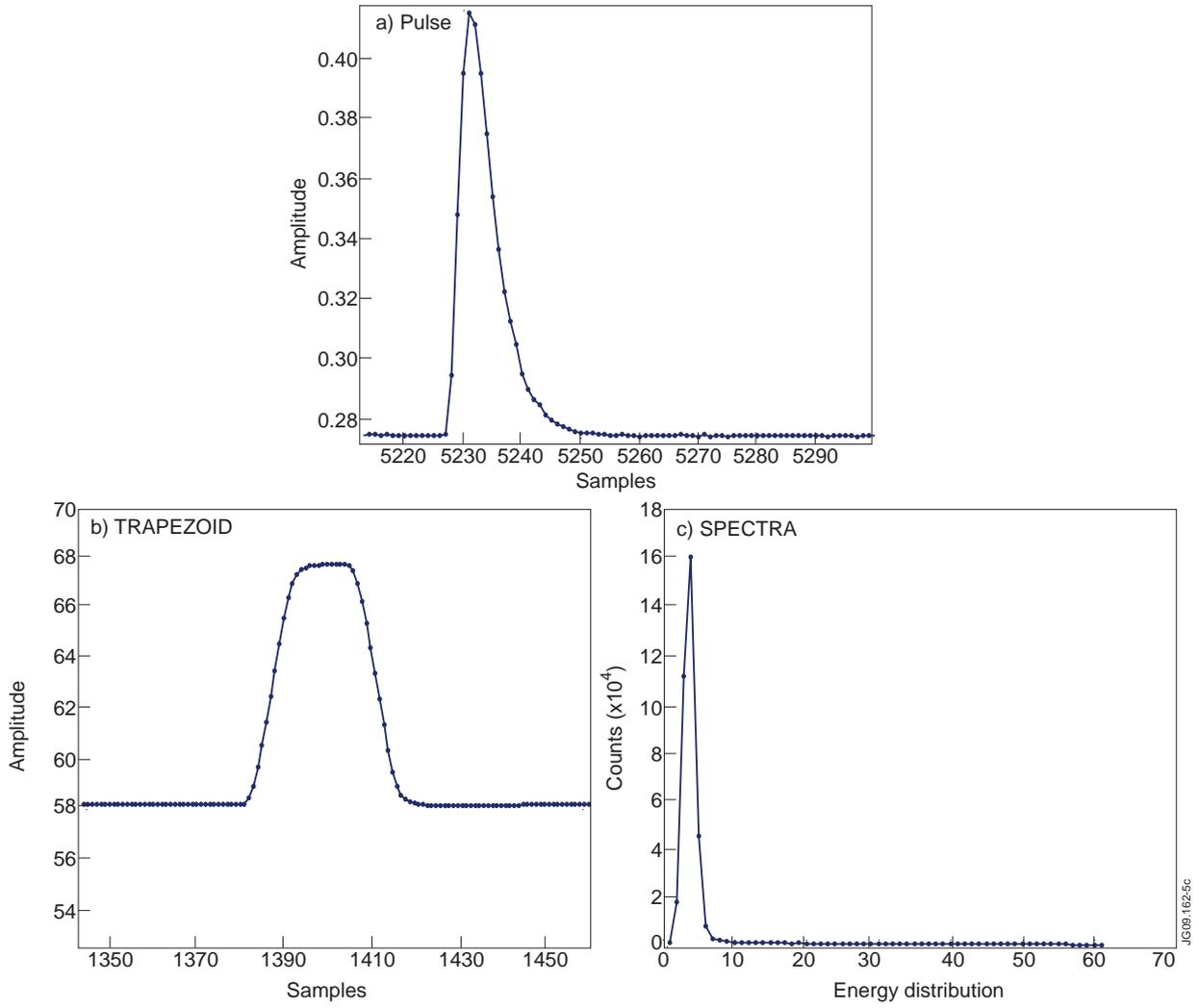


Figure 5: Results obtained with real time pulse processing algorithm inside FPGA, using acquired raw data with single energy amplitude plus noise, stored in AWG420 and sampled at 200MHz: a) Pulse event; b) Corresponding trapezoidal shape ($k=8, l=24$); c) Spectra build with 400k E_r values.