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** See annex of J. Pamela et al, "Overview of Recent JET Results and Future Perspectives", Fusion Energy 2002 (Proc. 19th IAEA Fusion Energy Conference, Lyon (2002)).*

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ABSTRACT.
This paper describes the hardware and the software structure of a new controller for the JET Error Field Correction Coils (EFCC) system, a set of ex-vessel coils that recently replaced the internal Saddle Coils. The EFCC controller has been developed on a conventional VME hardware platform, using a new software framework recently designed for real time applications at JET, and replaces the old Disruption Feedback Controller increasing the flexibility and the optimization of the system. The use of conventional hardware has required a particular effort in designing the software part in order to meet the specifications. The peculiarities of the new controller will be highlighted, such as its very useful trigger logic interface, which allows in principle exploring various error field experiment scenarios.

INTRODUCTION

Experiments about the stability of Resistive Wall Modes, error field induced locked modes and neo-classical tearing modes are routinely run on JET [1]. In some of these experiments, MHD instabilities are triggered by means of an external applied error magnetic field, which, in the past, was provided by a set of four Saddle Coils (SC) placed inside the vessel [2]. These coils were supplied by the Disruption Feedback Amplifier System (DFAS), a switching power amplifier consisting of four units rated for 3kA, 1kHz , or 1kA, 10kHz [3]. The DFAS is run in current control mode and in the past the load current reference signals were generated by the Disruption Feedback Controller (DFC) [2], designed to achieve feedback compensation of the MHD mode instabilities and to generate the current requests to the saddle coil power supplies.

The SC are going to be permanently disabled in-vessel during JET 2004 shutdown; in order to continue experiments on error fields and tearing modes a new system of Error Field Correction Coils (EFCC) has been installed externally to the vacuum vessel [4]. The EFCCs are supplied by the same DFAS which supplied the SC. To improve the flexibility of the new system and to integrate it in the JET new real-time applications framework, a completely new controller has been designed and implemented to replace DFC; the new controller is based on a VME standard hardware platform and on a new software framework for real-time applications, which is being used at JET also for plasma shape control [5,6]. This paper deals with the structure of this new controller, named EFCC Controller, focusing on the ability to generate reference signals up to 10kHz although the frequency of the control cycle is limited to 1kHz, thanks to a particular interrupt-driven algorithm; the trigger logic interface of the controller, which gives a great degree of flexibility to the system, will also be extensively described.

1. EFCC CONTROLLER DESIGN SPECIFICATIONS AND STRUCTURE

The constraints in the design of the EFCC Controller were associated mainly to the desired frequency of the output references for the DFAS and to the extreme flexibility required for the trigger logic. A major restriction was related to the necessity of limiting the system cost; as a consequence, only

conventional VME hardware immediately available at JET was used, transferring on the software side of the project the duty of achieving the specifications. As for the trigger logic, it is required that specific output reference signals of the new controller can be triggered by generic conditions, described by string of characters, involving available real-time measurements coming from the experiment.

The general principle structure of the EFCC controller is shown in fig.1. The EFCC Controller has to be able to generate four open-loop waveforms (one for each DFAS) up to 10kHz, which is the maximum rated frequency of the amplifiers. This means that the digital outputs of the controller have to be sampled at least at 100kHz, which is an extremely high value for conventional VME hardware and required a particular design of the software part. As for the input stage, in order to cope with the specifications related to the trigger logic, EFCC controller acquires an arbitrary large number of signals coming from the JET Real Time Data Network (RTDN), such as for instance the plasma current, the toroidal field, the neutral beam power, etc. A set of these signals is used to allow a feedforward compensation of the natural error field generated by the poloidal and toroidal circuit currents; a feedback section is also foreseen, based on four analogue signals coming from the pick-up coils placed inside the vessel.

2. EFCC CONTROLLER HARDWARE ARCHITECTURE

A general block scheme of the hardware arrangement is shown in fig. 2. Only conventional VME hardware has been used to limit the system cost. All analogue signals, four signals from the pick-up coils placed inside the vessel and four currents supplied by DFAS, are processed by a conditioning stage and then sampled by a VME data acquisition board (MPV956). The core of the system is a Motorola PowerPC (PPC), where the EFCC Controller tasks run. It is interfaced to the RTDN using the ATM (Asynchronous Transfer Mode) protocol and it communicates with the Control and Data Acquisition System (CODAS) of JET through an Ethernet connection. The central timing and triggering module (VPLS) provides the synchronisation of the EFCC controller with the JET central control by means of a VME software trigger every 1 ms. One single controller cycle is therefore 1 ms long; this value cannot be reduced. The choice of this hardware structure, driven by cost saving considerations, has led to a particular design of the controller cycle, which is shown in fig. 3. When a VPLS software trigger occurs, the 8 analogue signals coming from the conditioning stage are sequentially converted and stored into a FIFO memory by the MPV956. After a suitable time, data are collected by the controller software through the VME bus; the controller downloads only the first 8 samplings and resets the FIFO; calculations are performed in the next phase, which of course has to last less than 1ms. This method has been specifically chosen because it allows using standard VME hardware already available at JET, resulting in a consistent cost saving. As for the output stage, an output board provides digital to analogue conversion of the reference signals. The chosen board is not equipped with an output buffer memory, the output conversion is thus performed exactly when the PPC accesses the VME bus to send the waveform samplings to the output board; at 100kHz, the PPC, during each 1ms control cycle, has to access the VME bus every 10μs, requiring

a specific design of the EFCC Controller software; however, the solution is cheap; the complication has been transferred to the software part.

3. EFCC CONTROLLER SOFTWARE ARCHITECTURE

The EFCC Controller software architecture is based on the *JETRT* framework which is deeply described in [5]. The EFCC Controller software consists in a module integrated into the *JETRT* environment; the flexibility provided by the software framework and the massive use of object-oriented techniques allowed a relatively fast implementation of the controller functions. The most peculiar aspects of the controller are the trigger logic, the waveform generator and the synthesiser algorithm, which allows achieving the generation of high frequency waveforms although the frequency of the control cycle is limited to 1kHz and the output board has no buffer memory.

3.1 TRIGGER LOGIC

The basic idea behind the trigger logic structure is providing the possibility to trigger particular output waveforms whenever a certain condition or combination of conditions occurs. The conditions are codified strings of characters based on a set of input signals from the RTDN, a set of logical and mathematical operators and numbers; for instance "(IP > 3e6 AND TF < 1.2)", which means that, whenever the plasma current is greater than 3MA and the toroidal field is lower than 1.2T, a specified set of waveforms has to be generated. More complicated expressions are possible, giving a great flexibility to the system, that can be triggered virtually for whatever condition described by RTDN signals. The controller implements up to 16 experiment windows, each characterised by a start trigger condition, a stop trigger condition and a particular set of 4 waveforms to be generated. The experiment windows follow a priority order and their status (ready, armed, active, stopping, stopped) is determined by a finite state machine.

The trigger logic is implemented by means of classic parsing techniques similar to those commonly used in a language compiler. Input strings are processed by the trigger logic algorithm, which translates them in a proper logic network consisting of AND nodes and OR nodes. Inputs to this network are bits representing elementary conditions, while the output is a particular word whose bits represent the status of each start and stop condition. The state machine then manages the output and determines which experiment windows is active and what waveforms have to be synthesised.

3.2 WAVEFORM GENERATOR AND SYNTHESISER ALGORITHM

The EFCC Controller features a very flexible waveform generator able to synthesise almost any type of AC or DC waveform, with frequency and amplitude sweeps. The synthesis of a 10kHz AC waveform, given hardware structure, required forcing the controller to produce samplings at 100kHz; since the controller cycle time cannot be lower than 1 ms, a smart interrupt-driven synthesis has been used to overcome the problem, exploiting a particular feature of the PPC board that allows to generate VME bus interrupts at a selected frequency. Therefore, every 10μs (100kHz) an interrupt

is internally generated by the PPC and the associated Interrupt Service Routine acts as a synthesiser by generating the outputs on the basis of the requests coming from the controller. At the beginning of each control cycle, the controller calculates the new waveform parameters and updates the requests to the synthesiser. The structure of the synthesiser algorithm is schematised in fig.4.

CONCLUSIONS

The paper presented the hardware and software structure of the EFCC Controller. Although it is based on conventional VME hardware, the system is able to achieve the desired specifications in terms of waveform generations and trigger logic flexibility. The system has been successfully commissioned and operated during JET campaigns at the end of 2003; in particular, the open-loop generation of waveforms up to 10kHz has been verified and the trigger logic features have proven their usefulness. Thanks to these new features and to the possibility to easily upgrade or modify the system, the EFCC Controller will be a useful tool to perform error field and tearing modes studies on JET in the future.

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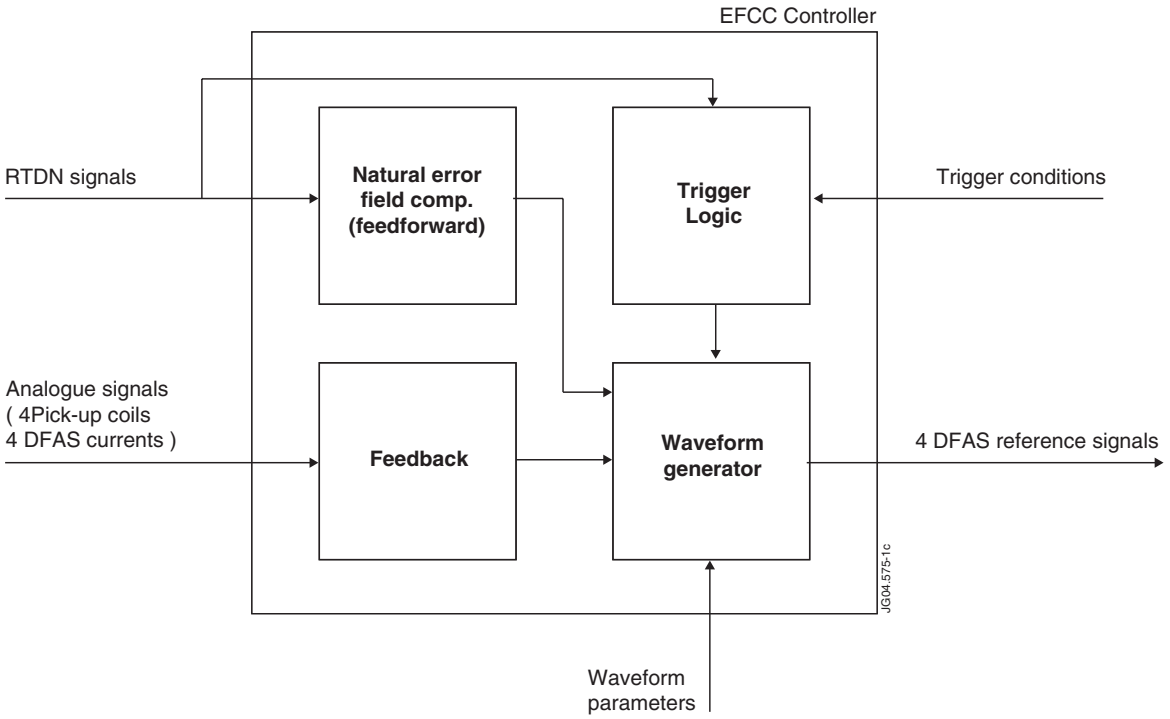

Figure 1: General structure of the EFCC controllor

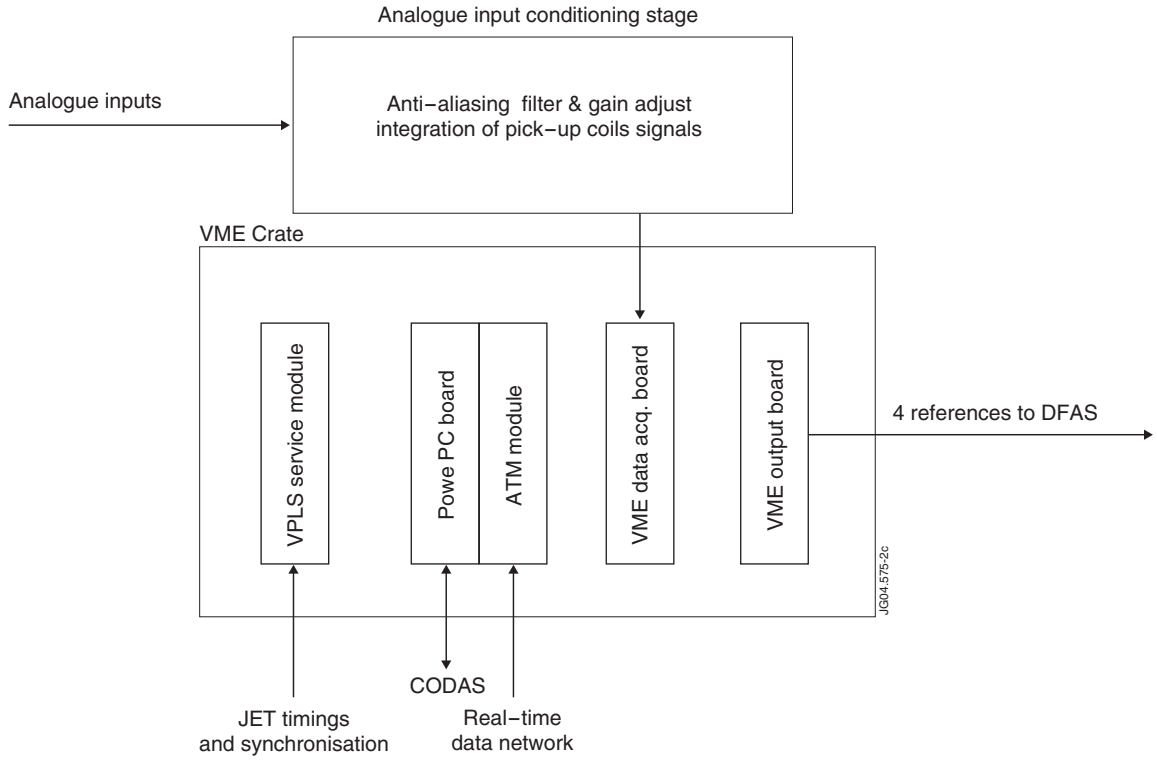

Figure 2: Scheme of the EFCC controllor hardware architecture

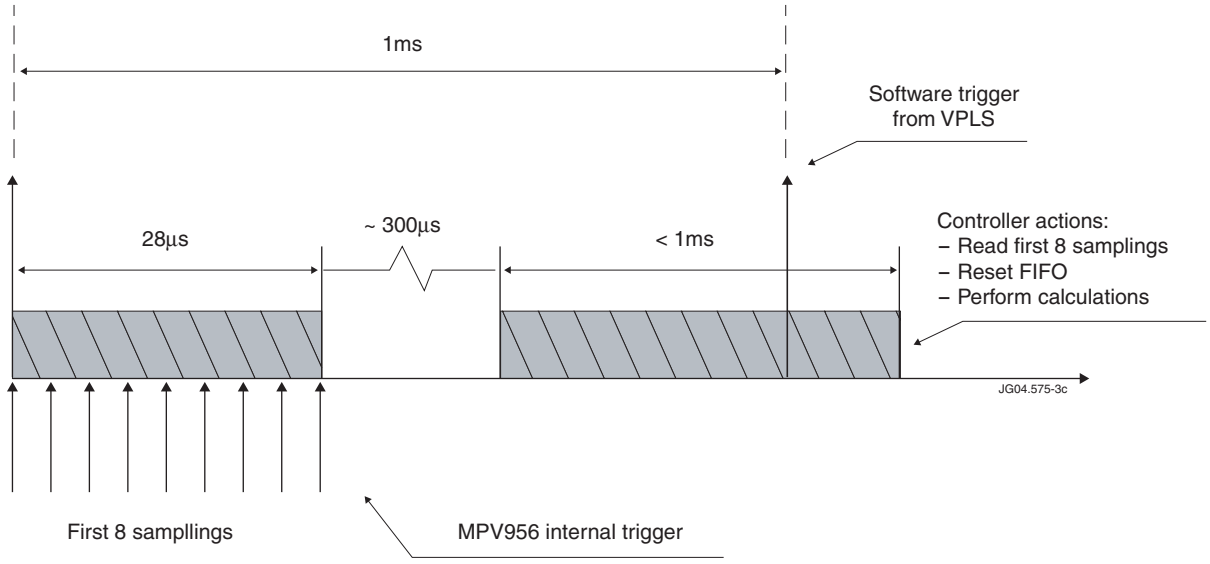

Figure 3: Sketch of the EFCC controllor control cyclye structure

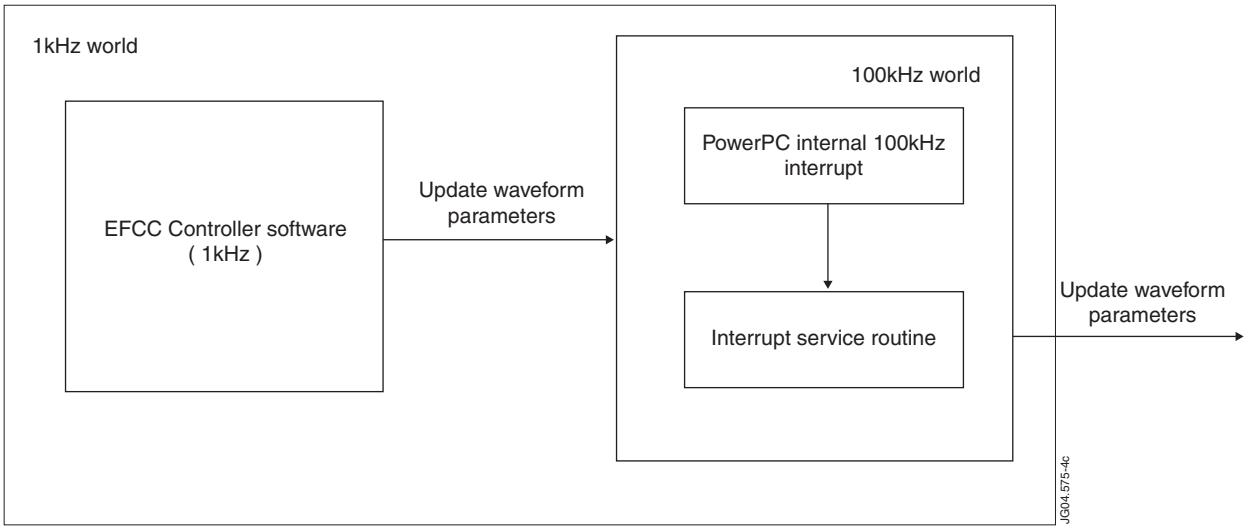

Figure 4: Structure of the synthesiser algorithm