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ABSTRACT.

The JET high triangularity (δ, HD) Divertor is an upgrade of the present JET divertor consisting of two modified toroidal segments which are: a new load bearing septum replacement plate (LB-SRP) tile located in the center of the divertor, and a High Field Gap Closure (HFGC) tile protecting inboard diagnostic cabling. The aim of the upgrade is to allow high power operation and a wider range of plasma triangularities at the divertor poloidal null. This paper describes the optimisation of the tile chamfering for LB-SRP and HFGC (including edge shadowing) and the power handling evaluation for a set of planned plasma configurations. The precise design of the tile faces is based on 12 plasma configurations given by the JET team, and on two sets of mechanical tile tolerances issued by the JET drawing office. The PROTEUS code (magnetic equilibrium by finite element) is used to calculate the various field line angles, which are inputs for the chamfering angle calculation process. After calculating the chamfering angle values of each face, a checking exercise has been realised on the 3D CATIA models of the tiles by putting them at their extreme tolerance positions and validating if the shadowing is ensured for a angle calculated to take into account the worst possibilities. With the final chamfering angle value for each face, the power handling of the tiles has been estimated with finite element calculations. Power handling is given either by the critical time to reach 1800°C at the tile surface for a total injected power of 40MW, or by the maximum total injected power allowable for a 10 second power pulse without exceeding 1800°C. The estimated power handling gives promising results in regard to the JET EP project objectives.

INTRODUCTION

The existing Mk II Gas Box divertor was modified by replacing the septum structure by a flat plate with no power handling capability. To increase the power handling capability at the outboard side, especially for plasmas at high triangularity, a new structure called Load Bearing Septum Replacement Plate (LB-SRP) will be installed in the Divertor during the 2004 shutdown. To improve the high triangularity capability at the inboard side of this divertor, a protection over the inboard gap has also to be added. This modified new divertor configuration is named Mark II HD, where HD means “high delta” (i.e. triangularity). The geometry of the divertor with these two tiles is illustrated on Figure 1. The global work to be conducted includes the design, procurement and delivery on site of the LB-SRP tiles (including a list of reference diagnostics) and of the High Field Gap Closure tiles (HFGC) which protects inboard diagnostic cabling. The task covered here is the optimisation of the chamfering of the tiles, carried out in order to ensure that the tile edges are protected from high power densities. For the demonstration of the performance, thermal calculations have been carried out for the reference configurations. These calculations use the wetted fraction and the temperature limit to estimate the power handling capacity of the divertor.

2. TILE DESIGN

2.1. MATERIALS AND PRINCIPLES

The LB-SRP and HFGC tile design is unidirectional: all tiles at a given major radius have the same slope in the toroidal direction, to hide any edge of the next tile from the impinging plasma. The tiles are machined from blanks of Carbon Fibre Composite (CFC) materials and are attached to the carrier via a dumb bell, yoke and disc spring pack system. In addition, the tiles are pre-compressed using tie rods, to avoid surface cracks due to temperature gradients. LB-SRP tiles are approximately 170 mm long in the toroidal direction, 260mm long in the poloidal direction, and 40mm thick. The material is a 2D CFC (Dunlop DMS704), with the direction of the fibres (i.e. of the high thermal conductivity) perpendicular to the surface and in the poloidal direction. HFGC tiles are approximately 150 mm long in the toroidal direction, 250mm long in the poloidal direction, and 27mm thick. The material is a needled 2D CFC (Le Carbone Loraine A035), with the direction of the fibres parallel to the surface. Metallic components (dumbbells, tie rods and disc springs) are in Inconel 718. Tolerances to be considered in the design process have been issued by the JET drawing office. For each tile, LB-SRP and HFGC, two set of tolerances are provided depending if the two tiles (adjacent in the toroidal direction) are on a common carrier or are on two different carriers.

On both sets of tiles the main design optimisation to improve power handling is the choice of the best chamfer tile chamfer angle that ensure the tile edges are protected from the impinging field lines for any design plasma scenario (high chamfer angle) while maximising the toroidal wetted fraction (low chamfer angle). Shadowing precisely the near perpendicular surfaces prevents the overheating of the edges and thus allows for a rapid plasma power ramp up with reduced out gassing and density control problems. The tile geometry optimisation is done for a set of 12 reference plasma configurations, 9 swept (named *1MA5_hd, 2MA5_hbhd, 3MA5_hd, 3MA5_ITER, 4MA_hd, 4MA_hd2, 4MA_hdhx, 4MA_hdlx, 5MA_hd*) and 3 static (named *"Extreme", H_4M5_LT and ICRH*), planned for the physics studies in the years following the installation of this divertor modification. The process for designing the LBSRP & HFGCP tile surface geometry aims principally at determining their poloidal and toroidal tilt. The following steps were done:

- A magnetic mapping of the divertor region was constructed with the "Proteus" code for the various plasma configurations. Combining the poloidal field map of the plasma scenario with the Toroidal Field (TF) distribution the code evaluates the local field line angles (θ_{para} & θ_{perp}) at any point of the divertor tile geometry.
- The distribution of θ_{perp} along the tile width (poloidal direction) is plotted for all configurations on the LB-SRP in Fig 2. The reference tile θ_{perp} is determined by choosing the straight line maximising all these angles. Consequently this angle is not constant along the tile. Moreover, it is then enhanced by a factor (Q95/2.3) for safety reasons on the plasma control.
- The edge shadowing is then adjusted to the various gap widths and tolerances (dissimilar tile adjustment between and within a carrier) by modifying one of the adjacent tile thickness which allows to keep a constant tile surface angle. A 1 mm safe length (chip allowance) is considered, but only on one tile (case of two defects facing each other is excluded).

2.2. LB-SRP DESIGN

The particular features considered for the LB-SRP design are the following:

- Variable chamfer angle (linear variation) identical for both tiles (on same or on various carriers)
- Optimisation of the tile chamfer angle calculation using the 2 sets of tolerances:

  Between carriers: X = ± 0.65 ; Y = ± 0.80 ; Z = ± 0.40 mm

  Common carrier: X = ± 0.15 ; Y = ± 0.15 ; Z = ± 0.10 mm
- The tile protecting the inter-carrier gap is thicker
- The tiles are not protected against reverse fluxes
- The Inner and the outer faces are tilted to protect the corners (only the inner face sees field lines but the outer is also chamfered because low values of θ_{para} could affect the shadowing of the corner)

Results for the main face, in terms of chamfering angle (α) and thickness variation (ΔT) are:

- Alpha varies linearly between inner and outer corners following a straight line equation which gives: At the upper inner corner, where the radius R is 2.57396 m, $\alpha = 0.5101°$
  At the lower outer corner, where the radius R is 2.81207 m, $\alpha = 0.8664°$
- Tile thickness increase for the second carrier tile (shadowing the inter-carrier gap): $\Delta T = + 0.210$ mm

2.3. HFGC DESIGN

The particular features considered for the HFGC tile design are the following:

- Single chamfer angle (all along the face) common for all tiles, calculated using the worst set of tolerances (Between carriers: X = ± 1.15 ; Y = +0.5/-1.25 ; Z = ± 0.35 mm), and two different gaps (13 and 42mm)

- Outer faces (upper and lower) are tilted to protect the corners

Results for the main face, in terms of chamfering angle (alpha) and thickness variation (ΔT) are:

- Main face: $\alpha = 1.746°$, thickness increase for shadowing the fixation hole: $\Delta T = + 1.28$mm, maximum tile thickness: 27mm
- Outer upper vertical face: $\alpha = 1.46°$, poloidal length increase for shadowing the fixation hole: $\Delta P = + 0.64$mm
- Outer lower vertical face: use of the same features than for the upper vertical face ($\alpha = 1.46°$), the tile length increase is not necessary.

2.4. FINAL CHECKING

Calculation of chamfering angles being performed on discrete results given by the Proteus code, there is an obvious concern that an error in the design could pass un-noticed. For these reasons, a checking process of the front faces of the tiles, developed in 1994 in order to check the final models

of the MKIIA tiles plasma faces, has been applied to verify that the worst possible combination of tolerances and flux can neither illuminate a tile edge, nor cast an excessive shadow. The exercise consists in calculating a check angle taking into account the worst possible perpendicular field line angles and applying it on a 3D CATIA model of the tiles put at their extreme tolerance positions to check the shadowing. This final checking exercise has been successfully performed for the MK II HD new tiles.

3. POWER HANDLING

3.1 – PRINCIPLE

The injected power is conducted to the divertor along the scrape of layer (SOL), which we assume has a thickness, λQ = 5mm, at the outer midplane. Given the final local geometry of the divertor tile (toroidal & poloidal), and the local field line angles, the heat flux distribution is evaluated by assuming a power repartition between inner and outer target and an intensity inversely proportional to the flux expansion. The tile wetted fraction is determined by the local angles for each configuration. Strike point sweeping (4Hz) was considered to enhance the power extraction for some specific configuration. For those swept configurations, an equivalent heat flux profile was calculated by integrating the flux distribution for the cycle. It was demonstrated in a 2D transient study [1] that the maximum surface temperature obtained with the equivalent profile was identical to that obtained from the detailed analysis. Thermal finite element calculations were done with a 1D model to obtain the pulse duration at full power when considering a 1800°C maximum surface temperature. The main assumptions of the power handling estimations are the followings:

- The critical time is the time to reach 1800°C at the tile surface for a total injected power of 40 MW (70% convected to the divertor: 28MW), and:
  - LB-SRP tile: inboard/outboard power sharing: 2.5/3.5 so 20MW on the outer leg,
  - HFGC tile: inboard/outboard 1/2 power sharing corresponding to the case of reverse field operation: 14MW on the inner leg.
- λQ = 5mm in the SOL and a decrease of power in the Private Flux Zone considering λQ /3.
- All calculations are 1-D, taking into account:
  - LB-SRP tile: a 40mm-thick Dunlop tile with lower conduction in the toroidal direction,
  - HFGC tile: a 23mm-thick A035 tile, with the bad conductivity in the thickness direction.
- Toroidal Wetted Fraction (TWF) is calculated point by point (particularly influent in the LB-SRP tile where the alpha varies along the tile profile),
- the effect of bowing has been assessed by comparison with a previous divertor study [1].
- the effect of Reverse flux is not taken into account (but some estimations have been made).
- For swept configurations, the incident flux considered for the thermal calculation is the maximum value of the average flux obtain in each point during the sweeping.
- For static configurations, the incident flux considered for the thermal calculation is the maximum value of the peaked static flux, but the critical time is corrected in order to take into account the difference between a flat and a peaked flux profile. Considering the very short critical times

obtained with the nominal power, the results for the static configurations are presented in terms of maximum total injected power allowable for a 10 seconds run, but the correction constant/peak flux is also taken into account.

3.2. RESULTS

The results for LB-SRP tile for swept and static configurations are respectively given in tables 1 and 2. Except for the "Extreme" configuration, which will have a limited critical time on HFGC tile (about 2 seconds, but already higher than the critical time for the LB-SRP for this configuration), no power handling limitation due the HFGC tile is expected.

SUMMARY AND CONCLUSIONS

Chamfering angles for the new LB-SRP and HFGC tiles of the MK II HD divertor have been calculated, optimised and checked in order to insure a good shadowing of the edges for each of the 12 reference plasma configurations. The consequent power handling has been estimated and gives promising results in regards to the JET EP project objectives.

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DISCLAIMER

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REFERENCES

[1] J-F. Salavy & al., "Final report on tile design for the Mark IIA-HP divertor in the framework of the JET-EP project", CEA Report, SEMT/BCCR, August 2002

Table 1: Swept configurations LB-SRP tile power handling

Configuration	Flux (max av.)	Critical time
1MA5_hd	10.2 MW/m†	7.6 s
2MA5_hbhd	8.7 MW/m†	10.3 s
3MA5_hd	6.8 MW/m†	15.9 s
3MA5_ITER	9.8 MW/m†	8.2 s
4MA_hd	7.0 MW/m†	15.3 s
4MA_hd2	6.5 MW/m†	17.7 s
4MA_hdhx	6.1 MW/m†	19.3 s
4MA_hdlx	8.3 MW/m†	11.4 s
5MA_hd	9.7 MW/m†	8.4 s

Table 1:
Swept configurations LB-SRP tile power handling

Table 2: Static configurations LB-SRP-tile power handling

Configuration	Allowable total power for a 10 s run	Critical time (40 MW)
1MA5_hd	13.9 MW	~ 1.2 s
2MA5_hbhd	32.4 MW	~ 8 s
3MA5_hd	21.8 MW	~ 3.2 s
3MA5_ITER	17.2 MW	~ 2 s
4MA_hd	23.1 MW	~ 4 s
4MA_hd2	23.4 MW	~ 4 s
4MA_hdhx	9.3 MW	~ 0.5 s
4MA_hdlx	34.5 MW	~ 8.5 s
5MA_hd	25.9 MW	~ 5 s
Extreme	7.2 MW	~ 0.2 s
H_4MA5_LT (*)	19.8 MW	~ 3 s (*)
ICRH (*)	22.0 MW	~ 3.5 s (*)
(*) for these two configs, the reverse flux at the inner part of the LB-SRP front face is very important		

Table 2:
Static configurations LB-SRP-tile power handling

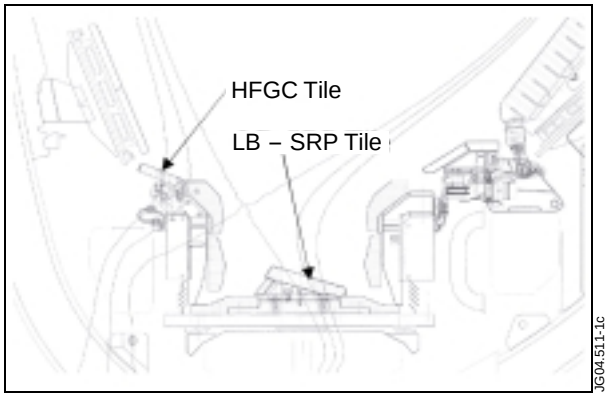

Figure 1: Poloidal section of the MKII GB Divertor with the new tiles (LB SRP & HFGC)

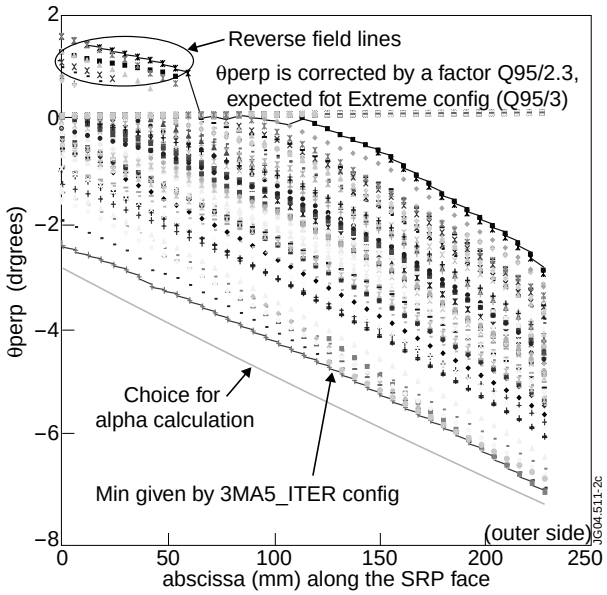

Figure 2: Distribution of qperp along the LB-SRP tile width (poloidal direction) for all configurations.