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** See annex of J. Pamela et al, "Overview of Recent JET Results and Future Perspectives", Fusion Energy 2002 (Proc. 19th IAEA Fusion Energy Conference, Lyon (2002)).*

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ABSTRACT

The company JEMA has delivered to the Joint European Torus (JET facility in Culham) two High Voltage Switching Mode Power Supplies (HVSMPS), each rated 130kVdc and 130A. One HVSMPS feeds the grids of two PINI loads. This paper describes the main control issues and the algorithms developed for the project.

The most demanding requirements, from the control point of view is an absolute accuracy of +/- 1300V and the possibility of performing up to 255 re-applications of the high voltage during a 20 second pulse.

Keeping the output voltage ripple to the specified tolerance has been a major achievement of the control system. Since the output stage is formed of several modules (120) connected in series, their stray capacity to ground significantly influences the individual contribution of each single module to the global output voltage. Two complementary techniques have been used to balance the effects of the stray capacities.

The fast re-applications requirement has a significant impact on the intermediate DC Link. This section is composed of a capacity of 0.83 Farad, which feeds the 120 invertor modules The DC Link is fed by a 12 pulse SCR rectifier, whose matching transformers are connected to the 36kV Grid. Every re-application and every voltage shutdown supposes a quasiinstantaneous power step of 17MWatt. Fast open loop algorithms have been implemented in order to keep the DC Link voltage within acceptable margins.

Moreover, the HVSMPS output characteristics have to be maintained during the rapid and important voltage fluctuations of the 36kV mains (28kV – 37kV).

The general control system is based on a Simatic S7 PLC, and a SCADA user interface. Up to 1000 signals are considered. The control system has demonstrated to allow for a rapid and accurate identification of faults and their origin.

INTRODUCTION

The main topology of the power supplies can be briefly described as follows (see figure 1). Two matching transformers adapt the 36kV of the grid to 670V. Such secondary voltage feeds a 12 pulse Thyristor converter, which provides a stabilised DC output at 650V. 120 IGBT invertor modules generate square shaped modulated waveforms at 2.7kHz from the common DC Link busbars at 650V. Each output of the IGBT invertors is connected to the primary of a High Voltage High Frequency (HVHF) transformer. The secondary voltages are rectified by means of fast diodes, in order to obtain an insulated DC component. The 120 diode rectifiers are connected in series in order to obtain the specified 130kV.

1. CONTROL OF THE THYRISTOR RECTIFIER

The control of the 12 pulse SCR rectifier has to achieve avery fast response in order to maintain the DC link voltage under acceptable values with changes of load from no load to 17Mwatt output in 150us and from full load back to no load conditions in 4us. Such transitions can be considered

quasi-instantaneous for a thyristor rectifier, since the one single control action can be taken every 1.67ms.

An additional difficulty is added by the 0.83 Farad capacitance, which, together with the impedance of the matching transformers creates a second order LC filter. Such topology naturally produces a DC current overshoot after every transition to full load. Feedforward techniques have been required in order to minimise such overcurrent peak.

A feedback loop and a feedforward algorithm are used in parallel. The feedback loop (Proportional – Integral PI controller) ensures the stability of the voltage while the feedforward part significantly improves the dynamic response.

In order to compensate for the voltage drop caused by the stray inductance, a lookup table with DC current input is used. This solution has been preferred to an alternative calculation, since the analytical expression gives poor performance in light load conditions, due to the effect of the thyristors loading the DC link capacity and not being able to discharge it.

The minimisation of the current overshoot associated with the transition from no load to full power is tackled by the so called 'modulation boost' algorithm.

The origin of the problem is that the energy is drawn initially from the capacitors and not from the SCR converter itself. The result is that the DC Link current transducer does not register any current until it is too late to take any controlling action.

Therefore, the following algorithm has been implemented:

- The instantaneous output power (equivalent to the real SCR rectifier output power) is calculated from the HV output voltage (Vout1) and output current (Iout1) signals
- A theoretical DC link current is estimated by dividing the calculated output power by the assumed 670V at the DC Link busbar.
- When an 'Inverter On' transition (equivalent from no load to full power transition) is detected, the modulation is taken to the maximum (modulation boost), until the feedback DC Link current reaches the value of the theoretical DC Link current.
- When the last condition is met, the modulation is taken to its normal value.

Such technique has proven to be effective and the DC link voltage is kept between 550V and 700V under worse case conditions, without triggering any protection.

Additional features of the SCR rectifier control include supply-line voltage compensation, a ramp generator and an arc cosine conversion table.

2. CONTROL OF THE IGBT INVERTOR MODULES

The IGBT invertor modules control is responsible for:

- Ramping up in a pre-selected time, between 150us and 500us
- Maintaining the output voltage and producing a low voltage ripple, within the limits of +/- 1300V, during the flat top.
- Stopping the power supply in less than 7us.

The output ripple voltage reduction has been the most challenging part. Therefore, it will be discussed in greater detail.

Theoretically, since the 120 IGBT converters modulate at 2778 Hz and a 3 electrical degrees phase shift between modules has been introduced, all the harmonics with frequency lower than 6667kHz (i.e., 2778Hz x 2 x 120) should be cancelled. Such hypothesis is not fully true, due to the effect of the parasitic capacities of the secondaries of the HVHF transformers and the diode rectifiers. Such capacities have a different contribution in elements located at different potentials. Since we are working in high voltage, the effect is not negligible and the asymmetry creates a first harmonic component at 5556Hz.

2.1 SELECTION OF AN OPTIMUM FIRING SEQUENCE OF THE 120 IGBT MODULES

Each of the 120 output stages cannot be considered equivalent from the point of view of its dynamic behaviour. For example, when invertor #1 is energised (connected to the grounded side of the output), the resulting voltage increment appears across the capacitances to ground of all 120 isolation transformers, in contrast to the situation for invertor #120 (at the opposite end of the stack) where the voltage increment only appears across the capacitance to ground of transformer #120.

Any asymmetry effect which is correlated with the physical position of the invertor or isolation transformer within the stack introduces a source of ripple which can be ameliorated by optimisation of the invertor firing order, defined by the sequence (i.e. firing order list) m(n), n=1, 2, … N, for N=120 (the total number of invertors). The optimisation may be achieved by grouping the invertors into L groups of K invertors (with KXL = N and K ≈ L; e.g. K = 10, L = 12).

i.e. $m(n) = g_j(i)$ $(j = 1,\ldots L;\ i = 1, \ldots K)$

where $g_j(i) = i^{th}$ member of the j^{th} group

with $n = (j-1)K + i$

In the above, the firing sequence runs through all the members of the first group, then through the second group etc.

The largest contribution to the ripple attributable to asymmetry effects occurs when one of the invertors energised at a particular time is replaced by another located at the opposite end of the stack. A first level of optimisation is obtained by ensuring that an exchange of invertors far apart in the physical stack ordering is guaranteed to occur within the shortest time interval, for all values of the modulation ratio. A sufficient condition for this is:

$$m(n+1) + m(n) \approx N (n = 1, \ldots N-1)$$

$$\text{and } m(N) + m(1) \approx N$$

In this case, the exchange of widely separated pairs of invertors will take place within one step of

the firing sequence, 3ms, so that the largest component of the asymmetry-induced ripple is shifted into the highest frequency harmonic and is effectively filtered out by the external circuit.

This required condition can be conveniently met by choosing the ith member of the jth group gj according to:

$$g_j(i) = h_j + (k_i - 1)\acute{}L$$

where $hj = j$

and $k_i + k_i + 1 \approx K$
$(i = 1, \ldots K\text{-}1)$
$k_K + k_1 \approx K$

for ki chosen from the set $\{1, 2, \ldots K\}$ in a suitable order.

e.g. $\{k_i\}$ could be taken as the ordered set {1, 9, 3,
7, 5, 6, 4, 8, 2, 10}
(for i = 1, 2, … K; K=10)

so that for this example of the choice of {ki}, the groups become the ordered sets:

$\{g_1(i)\} = \{1, 97, 25, 73, 49, 61, 37, 85, 13, 109\}$
$\{g_2(i)\} = \{2, 98, 26, 74, 50, 62, 38, 86, 14, 110\}$
.
.
$\{g_{12}(i)\} = \{12, 108, 36, 84, 60, 72, 48, 96, 24, 120\}$

which defines the firing sequence to be:

m(1)=1, m(2) = 97, m(3)=25, …, m(118)=96,
m(119)=24, m(120)=120.

The lowest frequency component of the output at constant modulation ratio is related to the time for the firing sequence to complete one entire cycle around all N modules before repeating i.e. 5.56kHz, twice the fundamental invertor frequency taking into account the fact that the rectified output of a given stage produces two pulses per cycle. A residual component of ripple at this frequency from asymmetry effects will remain if there is a systematic difference between invertor physical positions of the members of one group compared with the positions of the corresponding members of another group. This is the case when the members $g_j(i)$ are derived from a 'base' value hj, as above, which depends explicitly on j. This can be overcome by choosing instead the members $g_j(i)$ of the j^{th} group according to:

$$g_j(i) = h_j,i + (ki - 1)XL$$

where $h_j,i = \text{Random}(1, 2, \ldots L)$ for every j, i

whilst imposing the constraint that each $g_j(i)$ is unique.

Introducing such a degree of randomisation into the selection of the groups of invertors eliminates the systematic dependence of asymmetry effects on group identity and it significantly reduced the residual lowfrequency (twice fundamental) ripple, while still retaining the desired characteristic of shifting the largest ripple contribution from asymmetry effects into the highest frequency harmonic.

3.2 DYNAMIC COMPENSATION OF THE RIPPLE

The dynamic compensation algorithm is required because a traditional feedback loop controller does not achieve a fair efficiency. This is due to the important delay present on the transfer function.

This algorithm takes advantage of the repeatability of the output voltage ripple (5556Hz unaltered), which is synchronised with the invertor modules.

A period of 180us is divided into 8 segments of 22.5us. The average voltage during one segment is compared to the average value of the full period (180us). If the average voltage during the segment is higher than the average value of the period, a 'negative compensation' digital command is issued. In the opposite case, a 'positive compensation' digital command is generated.

Every segment has an associated buffer of overmodulation (or under-modulation). If a 'negative compensation' command is received, the segment buffer is decreased. If a 'positive compensation' command is received, the segment buffer is increased.

The modulation rate of the invertors is modified during every segment, with the value of the segment buffer.

In figure 3, it can be observed how a very significant ripple reduction is achieved in only a few milliseconds. It has to be noted that the Proportional – Integral (PI) controller slightly changes its operation after the first 3ms. After such key time a filtered output voltage feedback is used instead of the instantaneous value. A digital comb filter is used for getting completely rid of the harmonics from 5556Hz on. Such filtered signal is efficiently used by the PI controller, in order to avoid interference with the compensation algorithm discussed above. Additional features of the invertor control system include a ramp generator and DC link voltage compensation.

4. GENERAL CONTROL SYSTEM

A Siemens S7 PLC is used for the general control system and diagnosis.

Up to 1000 signals have been used for efficiently identifying possible faults, both in time and location. This has proved to be especially important for rapidly locating and solving faults in any of the 120 invertors in every power supply.

The whole power supply is monitored in local mode from a SCADA interface. A front screen represents all the significant parts of the power supply and includes links for detailed diagnostics. The SCADA interface also includes online event display and stored waveforms of the most relevant analogue measurements.

The general control system interfaces with the JET interface rack by means of a Profibus link and digital TTL signals for exchanging the most critical information.

CONCLUSIONS

If appropriate control techniques are used, fast transient response and output voltage ripple minimisation can be achieved by means of active devices located at low voltage. This validates the proposed global solution for supplying critical loads at high voltage, with added advantages of low stored energy and intrinsic safety of the system**.**

This two power supplies, controlled as described on this paper, are fully operational on PINI loads [2].

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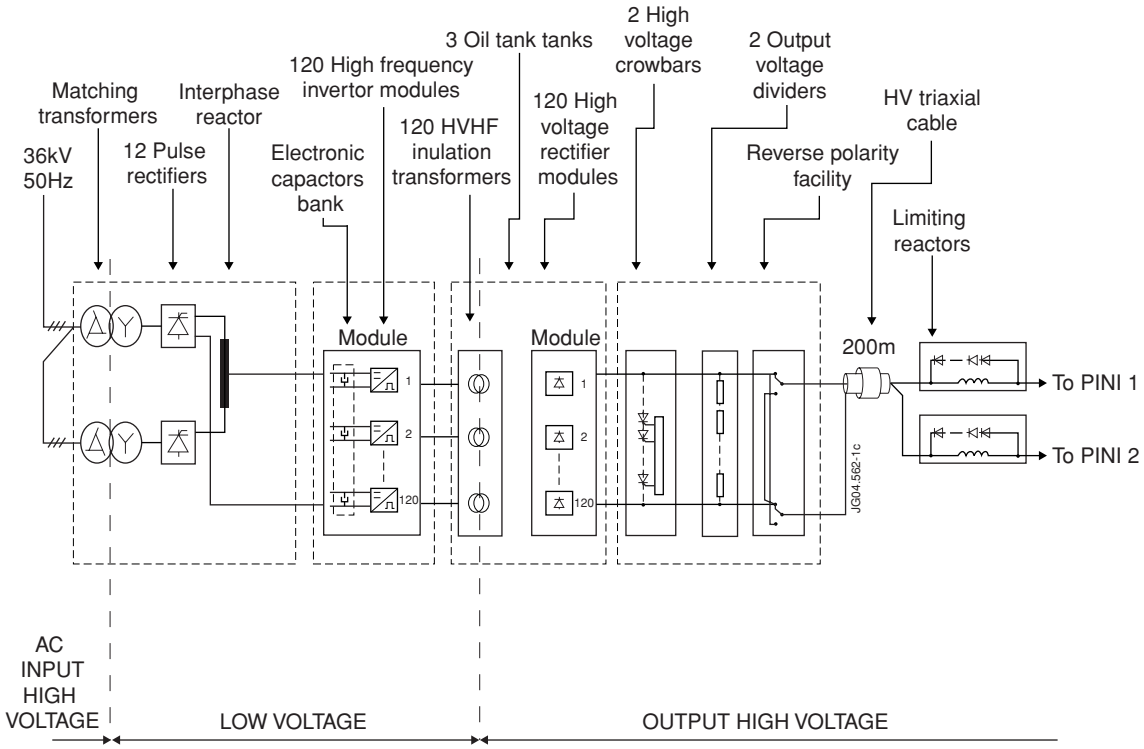

Figure 1: Single line diagram

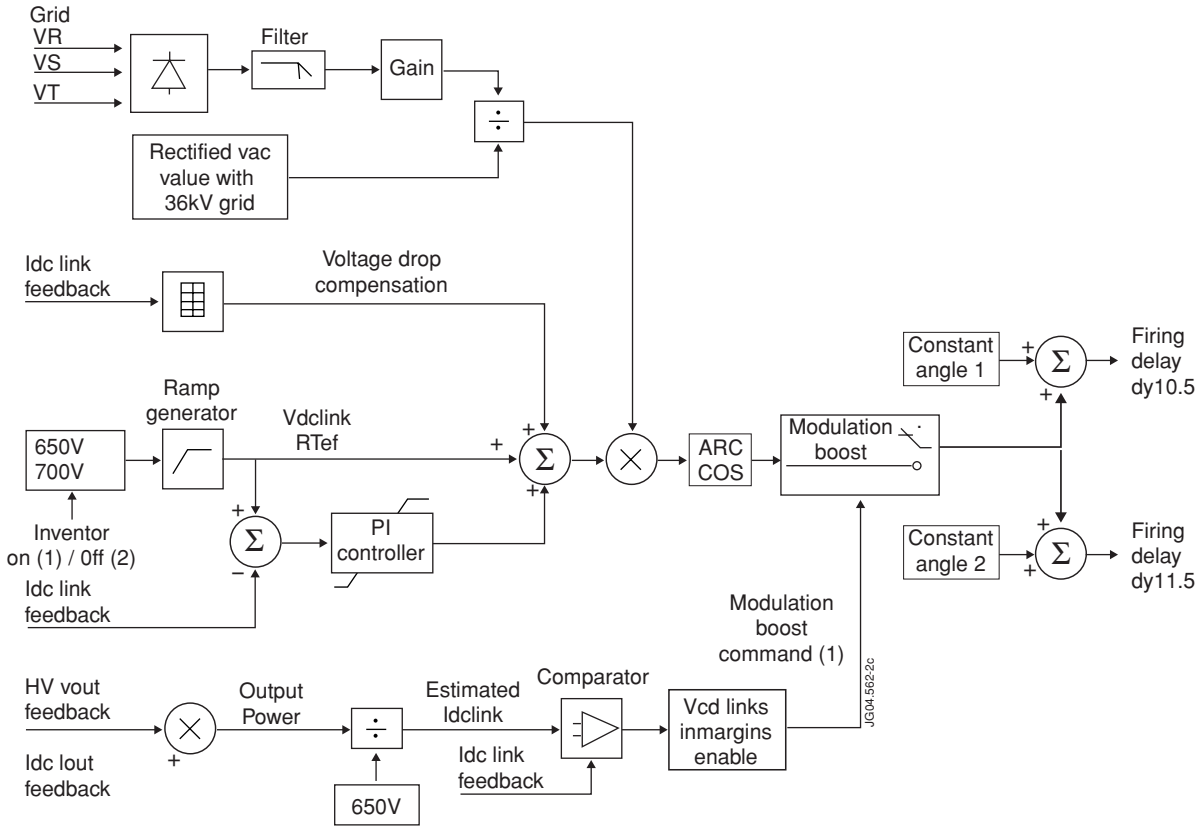

Figure 2: Control algorithm of the SCR Rectifier

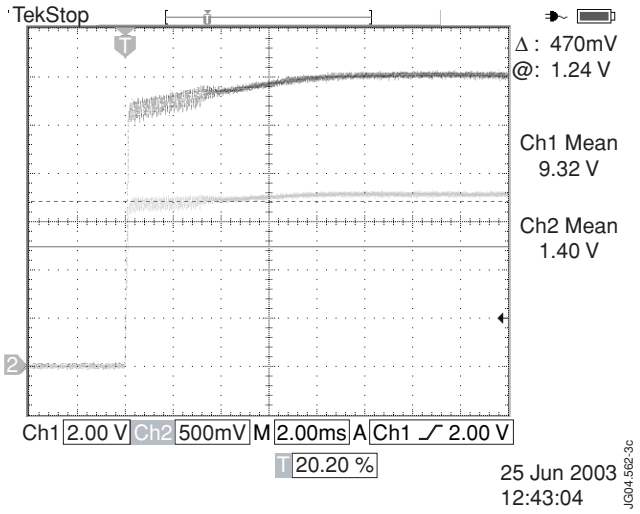

Figure 3: Ripple voltage reduction (CH1) after 3ms, at 120kV

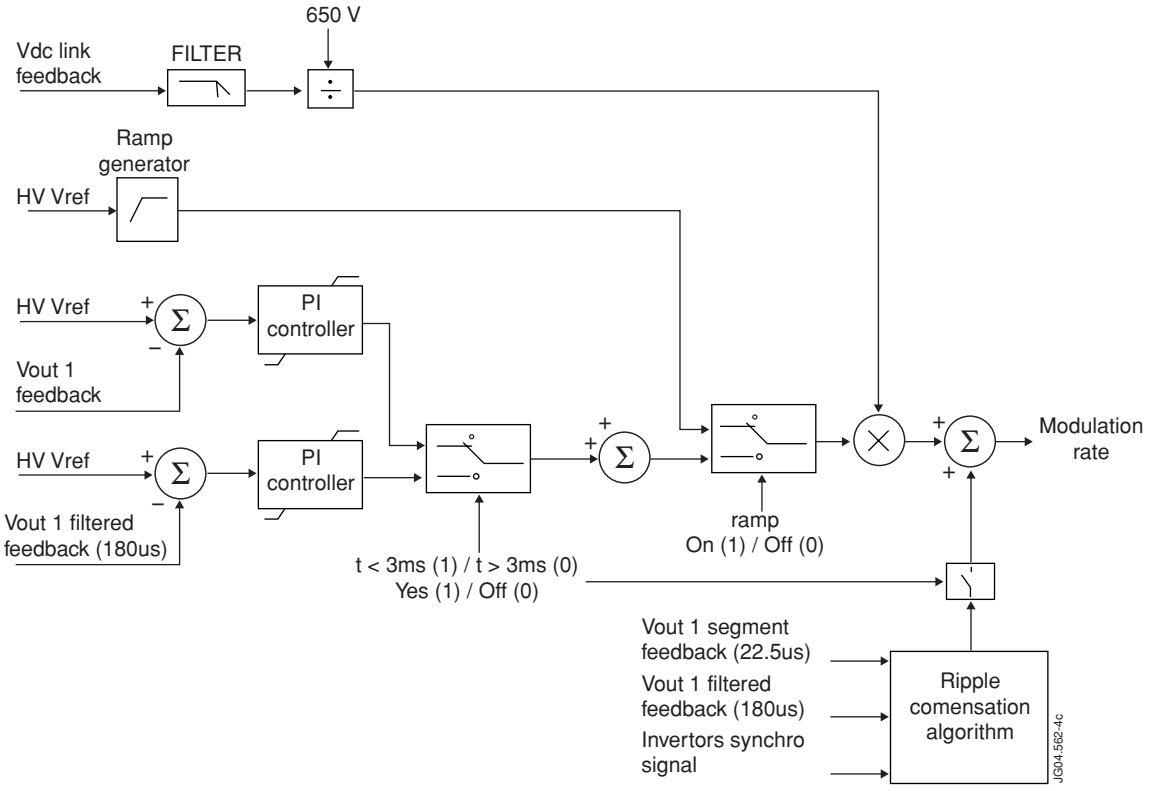

Figure 4: Control algorithm of the Invertor Control