EUROPEAN FUSION DEVELOPMENT AGREEMENT

EFDA–JET–CP(03)02-4

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** See annex of J. Pamela et al, "Overview of Recent JET Results and Future Perspectives", Fusion Energy 2000 (Proc. 18th Int. Conf. Sorrento, 2000), IAEA, Vienna (2001).*

Preprint of Paper to be submitted for publication in Proceedings of the
4th IAEA Conference,
(San Diego, California, USA 21-23 July 2003)

ABSTRACT

A PCI time digitizer module with eight independent Time-to-Digital Converter (TDC) channels is being developed for the new Time-of-Flight spectrometer designed for Optimized Rate (TOFOR) which diagnoses deuterium plasmas of the EFDA-JET tokamak. The module shall measure with high accuracy and resolution flight-times of 2.5MeV neutrons in the 100ns range as given by two groups of scintillation detectors operating at event rates up to several hundred kHz. To attain the requirements of the TOFOR, the time digitizer module was designed to handle a peak event rate of 1.25Gevents/s/channel and a sustained event rate of 5Mevents/s/channel. The digitizer time resolution and the dead-time between events are as low as 400ps. A maximum of 8 Mevents/channel can be stored in the 512Mbytes onboard memory and the time marks cover a period of up to 300 days. The module incorporates a Digital Signal Processor and a System-On-Chip device which performs the data transfer, the device control/monitoring and may perform statistical, data reduction or control algorithms in real-time. The high channel count, the implementation of the TDCs around a 2.5Gbit/s digital communications device and the use of common industry components, contribute to reduce the overall cost per channel.

1. INTRODUCTION

This paper describes a PCI [1] time digitizer module with eight Time-to-Digital Converter (TDC) [2] channels that is being developed for a time-of-flight spectrometer designed for optimized rate Time-Of-Flight measurements at Optimized Rate (TOFOR) [3]. The module shall measure, with high accuracy and resolution, flight-times of neutrons in the 100ns range as provided by two groups of scintillation detectors operating at event rates up to several hundred kHz. TOFOR is a new instrument for 2.5MeV neutrons to diagnose deuterium plasmas of the European Fusion Development Agreement - Joint European Torus (EFDA-JET) tokamak with the high accuracy that comes with the ability to operate at signal rates approaching the theoretical limit of the coincidence measurements (up to 0.5MHz for the application at hand).

To attain the TOFOR requirements, an innovative TDC was designed using a 2.5GHz communications interface. This approach allows a programmable resolution of 0.4 to 2ns and similar minimum time spacing between pulses in the same channel. All channels are independent and allow a peak event rate of 1.25 Gevents/s/channel and a sustained pulse rate of 5 Mevents/s/channel. The pulse occurrence time is coded into a 64-bit word permitting 8 Mevents per channel to be stored in the onboard memory. The time marks can span a period of up to 300 days. Channels may be grouped in order to improve the time resolution. Signals are provided for synchronizing up to five boards to increase the number of channels if needed.

The Digital Signal Processor (DSP) included in the module allows real-time control/monitoring and data processing. The DSP can run algorithms appropriate to the quantities being measured, permitting real-time execution of statistical, data reduction or control algorithms, besides the operation for long periods. The use of a System-On-Chip (SoC)(A highly integrated device composed

of multiple functional blocks, including on-chip memory and a processor.) Field Programmable Gate Array (FPGA) device complements the DSP capabilities and allows programmable logic changes to be implemented without the need for costly hardware modifications. This inboard DSP/FPGA combination can process the acquired events for real-time operations at an optimal data throughput. Other time digitizer implementations in the industry must use external DSP modules on the PCI bus (or the controller PC itself) for this task but are limited by the maximum throughput on the PCI bus.

The module has a low cost per channel since it provides 8 channels in one board, against a maximum of four on other industry modules and was designed using common industry components.

This paper presents the time digitizers with a description of the TDC module architecture including its front-end and pulse processor and provides a summary of its main characteristics. The module software is also discussed.

2. TIME DIGITIZER DESCRIPTION

2.1 TDC MODULE ARCHITECTURE

The hardware proposed for the time digitizer (Figure 1) is based on a PCI 2.2 board which includes a Texas Instruments® TMS320C64xx family DSP [4], a Xilinx® Virtex-II Pro FPGA [5], a Time-to-Digital Converter (TDC) front-end (Figure 2) and up to 512 MB of Synchronous Dynamic Random Access Memory (SDRAM) memory. This versatile architecture is readily reconfigurable to suit different applications as demonstrated before [6, 7].

In our application, the DSP controls simultaneously the PCI interface and the SDRAM memory and can also perform real-time digital signal processing. Very fast algorithms may be optionally applied to the input signals inside the FPGA. The host computer has Direct Memory Access (DMA) (method by which data is read or written from shared memory through a hardware proxy with minimal processor intervention) access to all memory space of the module including the SDRAM memory where the pulses and time data are stored.

The time digitizer module provides 8 TDC channels based on the Low-Voltage Positive Emitter-Coupled Logic(LVPECL) logic technology, sampling at the maximum rate of 2.5GHz. The time digitizers are started by software allowing the channels to generate time stamps for each input event. An external start pulse can be used to mark an absolute time reference. The foreseen duration of measurement for JET time-of-flight neutron spectrometer is about 20s which is well under the TDC maximum time span.

2.2 TDC FRONT-END

Most of the existing TDC designs are based on the CMOS integrated circuit technology characterized by a time jitter in the order of the hundreds of picoseconds thereby limiting the precision of the TDCs to a higher value. Recent implementations have better resolutions [8] but still use a common memory queue for the acquired data which limits the maximum pulse rate per channel. The LVPECL based Gigabit Communications devices integrated in an FPGA [9] can be used for the design of an innovative TDC (Figure 2) which has a resolution of 400ps and a time jitter of tenths of picoseconds.

This approach allows also grouping channels in order to improve the time resolution (e.g. a resolution of 50ps can be attained using eight 400ps input
channels) which may be desirable in some cases.

The TDC front-end operates in the following way:

1. Each channel contains a programmable level converter which translates the NIM or ECL input pulse levels to the board LVPECL levels.
2. The LVPECL pulses are input to one of the two inputs of an inverter gate; the other input is fed with a known serial sequence of 40-bit frames (each bit has a minimum period of 400 ps).
3. This sequence is generated by a 2.5Gbit/s digitally encoded data transmitter and fed synchronously to all inverters to serve as a common time reference to all input channels. Frames are counted to provide a time counter with a resolution of 16 ns (40 bit x 0.4 ns/bit). The 2.5GHz transmitter frequency is generated by a Phase-Locked-Loop (PLL) which multiplies an external 125MHz clock by 20.
4. Whenever a pulse occurs, the serial sequence polarity is changed allowing the detection of the pulse rise and fall time after decoding the frames later in the receiver. Each transition time in the frame is represented by a value from 0 to 15.6ns which will afterwards be summed to the frame time.
5. The asynchronously modified serial sequence is sampled by a 2.5GHz clock recovered from the transmitter output stream. Each channel has an associated Gigabit Data Receiver (GDR) which must receive a synchronous data stream without transitions uncertainty.
6. Each GDR will output a lower frequency parallel word every forty bits serial frame for subsequent lower-speed analysis in the FPGA.

A mechanism is provided to override the input pulses and transmit a special sequence to synchronize the receivers in the correct word boundary. The time value, relative to the start of the frame, of each inversion in any bit of the 40-bit word can be afterwards decoded with a resolution of 0.4ns inside the FPGA. Data will be processed separately for each channel thereby maximizing the pulse rate.

2.3 PULSE PROCESSOR ARCHITECTURE

The data flow of the pulse processor inside the FPGA is depicted in Figure 3. Each 40-bit output word from the receivers (RX) is available at a rate of one per 16 ns (at 62.5Mbit/s) in synchronization with the same 125MHz clock which was used to generate the 2.5Gbit/s transmit sequence.

The FPGA contains one 50-bit time counter which is incremented by a 62.5MHz clock, resulting from dividing by two the 125 MHz external clock frequency, to provide a wide time register common to all channels. The time counter value multiplied by 40 (56 bits maximum width), the 40-bit word plus the last previous bit and the 7 tag bits that indicate the channel where the event occurred, are input to a 104-bit wide First-In-First-Out memory (FIFO). This queue stores up to 511 words (with a maximum of 20 events per word) at the maximum rate of 1.25Gevent/s.

Subsequently a state machine decodes any level transition in the 41-bit words by generating a 6-

bit word for each transition edge time in the 41 bit frame (up to 40 words) plus 1-bit polarity and outputs a 64-bit word containing the 56 bits from the time counter summed with the 6 bits of fine resolution(The 56 bits used to express the time value of an event in the input allows a maximum time span of 2^56*0.4 ns ≅ 333 days), the polarity bit and the 7 tag bits. The time values (When storing both edges of the pulse the maximum hit-rate is halved. The application in hand will not need this feature) for the leading edge and trailing edges of these pulses can be selected for storage in a subsequent FIFO. An interrupt is issued to the processor whenever this memory is half-full allowing the processor to fetch the pulse time data through the DSP EMIF bus to the external SDRAM. The processor is fast enough (The DSP DMA/Interrupt mechanism transfers the digitized pulses in the FPGA queue to the DSP fast internal memory and afterwards stores it in the SDRAM memory) to move the half queue contents to the main memory before another interrupt is issued at the specified pulse rate. The queue depth is enough for storing 511 events from where they can be fetched at the maximum rate of 100 Mevents/s. An interrupt is issued to the DSP whenever pulses are discarded due to overflow on both FIFO queues. The STATUS REGISTER is used to identify the channels which issued the interruption. The pulse processor settings are configured trough the CONTROL REGISTER and the current time can be obtained reading the CURRENT TIME REGISTER.

2.4 MODULE CHARACTERISTICS

The innovative design of this module permits one to achieve some unique technical characteristics. In summary, these are:

- The minimum time interval between pulse transitions in the same channel (dead time) is 0.4ns.
- The pulse minimum width is 0.4 ns and there are no maximum width limits except the maximum time span.
- No dead time between pulses for any pair of channels.
- The average maximum count rate (direct storage in local memory without signal processing) is 5MHz/channel. When this value is exceeded and the queue is full the pulses will be discarded.
- The peak count rate is 1.25 GHz for a burst of up to 511 pulses.
- The time resolution is user programmable in 16 discrete steps from 0.4 to 2.0ns.
- The input time jitter is targeted to be less than 50ps.
- The time span is 2^56 x 0.4ns > 333 days.
- An external inter-board synchronization plug is incorporated in each board. The ECL synchronization lines allow time accuracies of the order of the TDC resolution when synchronizing two boards, if trimmed length cables are used.
- 50 Ohm input impedance and programmable input levels such as negative fast NIM (logic "1", -12 to -36mA, -16mA typ.; logic "0", -4 to 20mA, 0mA typ. – over 50ohm) or ECL.

3. SOFTWARE

The module device driver is being developed using the Windriver® development platform which is

portable to several operative systems. A C++ program portable to Win32 and Linux is also being developed to allow module testing, simple data visualization and statistics. Real-time control, visualization and algorithm programs can be developed for the DSP using the TI Code Composer Studio® IDE, uploaded to the DSP for debugging through a JTAG [10] cable and stored in the module Flash Electrically Erasable Programmable Read-Only Memory (EEPROM) for permanent use.

CONCLUSIONS

The low-cost, versatile and innovative architecture of the proposed module has been designed to meet present and future needs of the neutron diagnostics experiments; especially, functional changes can be made as demanded without requiring costly hardware modifications. The design permits also uncommonly high pulse rates and includes a high amount of fast on-board memory to support the operation of the experiments for long periods. Real-time operation and algorithmic calculations are supported inboard. A time digitizer with up to 24 input channels or resolutions of 100ps can be designed with powerful devices from the same FPGA family, which are now becoming available. In addition, using faster memory, it may reach an event rate of up to 20Mevents/s/channel.

ACKNOWLEDGEMENTS

The TOFOR Project is included in the JET Enhanced Performance Project and is being performed in a joint collaboration between the EURATOM Associations VR, ENEA/CNR-Milano and IST/CFN besides UKAEA as the JET Operator. This work has been carried out within the framework of the European Fusion Development Task Agreement (Contract JW2-TA-EP-TOF-01), with financial support from the European Communities and the JET joint fund. The views and opinions expressed herein do not necessarily reflect those of the European Commission and the EFDA Associates.

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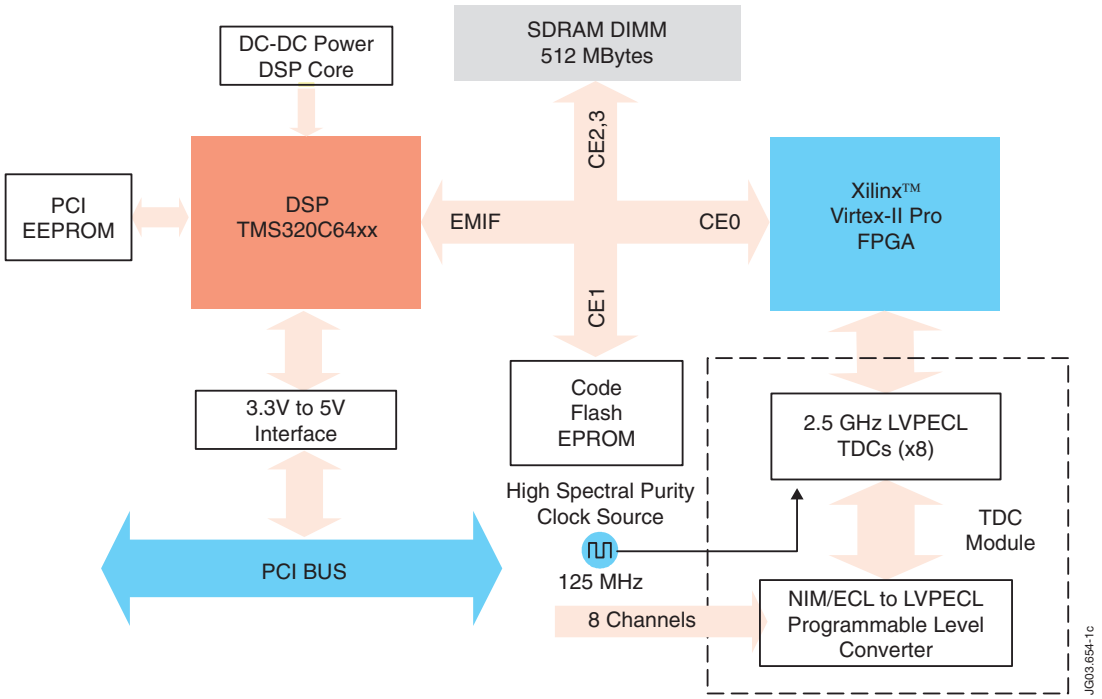

Figure 1: The time digitizer architecture.

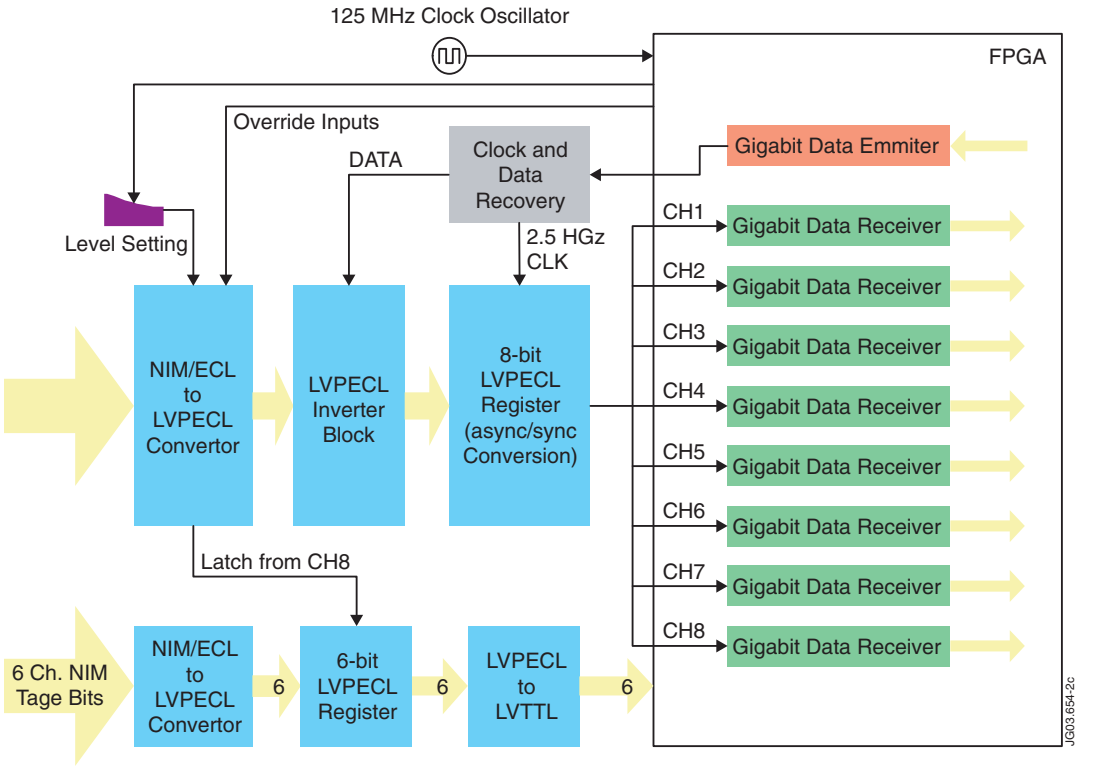

Figure 2: The 2.5 GHz PECL Time to Digital Converter.

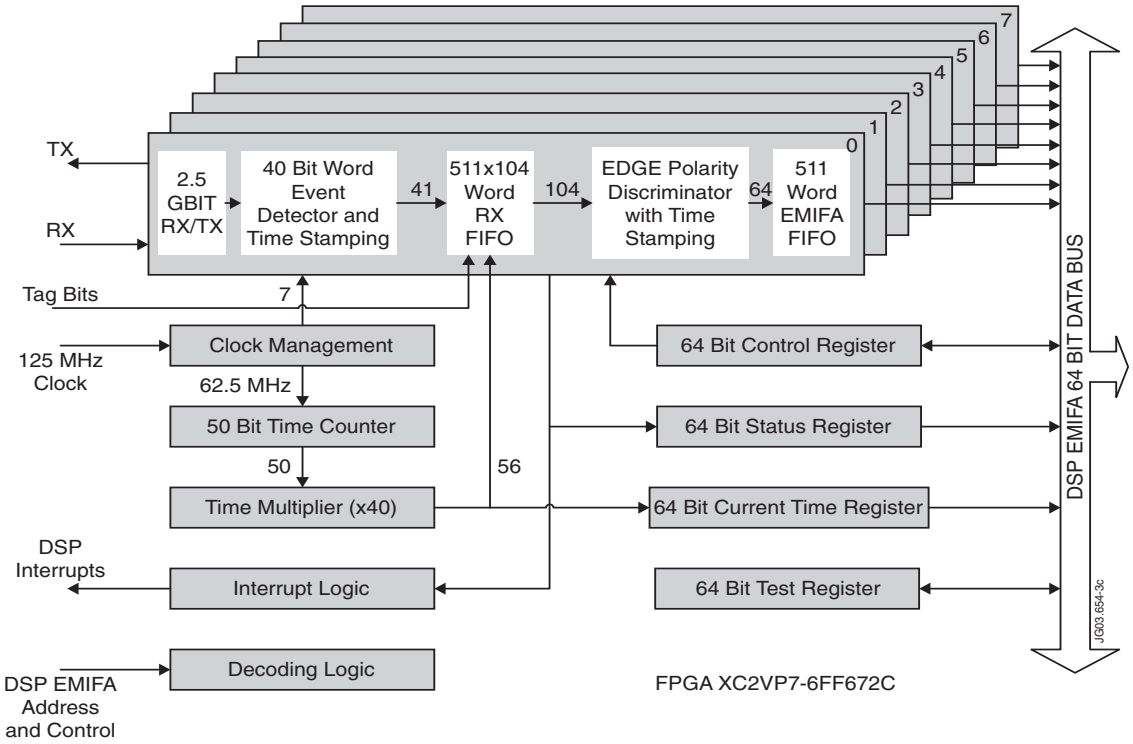

Figure 3: Pulse decoder flow on the FPGA.