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** See annex of J. Pamela et al, "Overview of Recent JET Results and Future Perspectives", Fusion Energy 2000 (Proc. 18th Int. Conf. Sorrento, 2000), IAEA, Vienna (2001).*

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ABSTRACT

A transient recorder module is being developed as part of the upgrade for the magnetic proton Recoil Neutron (MPRu) spectrometer for the JET Enhanced Performance Project. The MPRu will use a 32-channel focal plane detector with laminated scintillators of the so-called Phoswich type each read out by two PM tubes. The new detector will enable increase of the measurement sensitivity by several orders of magnitude compared with the present system. To attain the specific requirements of this diagnostic, a new PCI 200 MSPS transient recorder module with four independent Analog-to-Digital Converter (ADC) channels was developed. The module includes a Texas Instruments® TMS320C64xx family Digital Signal Processor (DSP), a Xilinx® FPGA and an ADC front-end. An inboard memory buffer implemented with up to 512MB allows the acquisition for large periods. Real-time digital signal processing algorithms can be applied to the input signals in the FPGA and the DSP. Multiplatform device drivers and a visualization program were developed to access the module memory where the pulses and time data are stored.

1. INTRODUCTION

This paper presents a new transient recorder module developed for the Magnetic Proton Recoil Neutron (MPRu) spectrometer as part of the JET-Enhanced Performance Project. The MPRu will use a 32-channel focal plane detector with laminated scintillators of the so-called Phoswich type each read out by two PM tubes. The main purpose of the new focal plane detector and accompanying electronics is to increase the measurement sensitivity by many orders of magnitude compared with the present system [1]. The MPRu will allow 2.5- and 14-MeV neutron emission spectrometry diagnosis of both D and DT and serves as a prototype for developing instrumentation for ITER.

To attain the specific requirements of pulse shape digitization for this diagnostic [2], a new 200-MSPS transient recorder PCI board with four independent 8-bit Analog-to-Digital Converter (ADC) channels was developed. The board should provide capability for large pulse shape storage of incoming events at high rate with accurate time correlation.

The developed module has an innovative architecture capable of multiple applications [3][4], with minimum hardware modifications and uses recent technologies in digital signal processors and programmable logic.

This paper contains a description of the transient recorder that details the module architecture, the digitalization timing of pulse shapes, and the data flow and processing besides the main performance characteristics and the module software.

2. MODULE ARCHITECTURE

Figure 1 presents the module architecture which is based on four free-running Analog to Digital Converter (ADC) channels directly attached to a Field Programmable Gate Array (FPGA) of the VirtexII-Pro™ family (XCV2P7) [5] from 1 Analog to Digital Converter. 3 Xilinx™, where data is buffered, validated and stamped. As data is becoming available on the temporary memory buffers

inside the FPGA, a Digital Signal Processor (DSP) of the TMS320C64xx™ Texas Instruments® family (TMS320C6415) [6] provides real-time data transfer into the local Synchronous Dynamic Random Access Memory (SDRAM). The DSP also controls the access to the stored data by the host through the embedded Peripheral Component Interface (PCI) master/slave interface controller which is compliant with PCI rev.2.2 [7]. Xilinx™ FPGA VirtexII-Pro XCV2P-7™ TI®

Figure 2 presents the FPGA architecture of the module. It provides rich trigger capabilities with flexible pulse parameters definitions and allows recording the occurrence time of the pulses. A high speed control and data transfer interface to the DSP is also provided. The following sections 2.1 to 2.6 detail the functional blocks of the module.

2.1 ADC CHANNELS AND TIMING

The module provides four independent single-ended channels with an input voltage range of -5V to 0V over 50W. Each channel of the ADC (ADC08200 from Analog Devices® which runs at 200 Mega Samples Per Second (MSPS) has eight bit resolution. To achieve high accuracy, low noise and to minimize skew between channels special care was taken on the analog power distribution and on the 200MHz ADCs clock distribution. The preliminary tests indicate good performance as shown in Figure 3 where pulse data acquired by a Tektronix® digital oscilloscope (TDS7104, 1GHz Bandwidth @ 10 GSPs) (top panel in Figure 3) and by the module (bottom panel in Figure 3), using an ascending trigger at -2.5V with a pre-trigger of 7µs and pulse duration of 10µs (2000 samples), are compared and confirmed to be similar.

2.2 TRIGGER BLOCK

The trigger block is independent for each acquisition channel and is composed of two parts (Figure 4), namely, the digital trigger detection and the trigger/storing control. The digital trigger detection is made by simple digital comparison of a single sample or sliding averages of two, three or four samples with a user defined value ranging from 1 to 254 (–19,6mV to –4,98V). A Schmitt-trigger detection circuit is currently under development. Features for user selection of between ascending or descending curve triggering and the disabling the trigger detection for a period ranging from 20ns up to 5.12µs after a valid trigger are also present.

The Trigger/Storing Control (TSC) block manages all channel trigger sources and generates reference control signals for storing the pulses and their parameters in the Secondary Buffer (SB) and in the Pulse Parameter Recorder (PPR), respectively. The possible trigger sources are a software accessible register bit, the digital trigger circuit and an external TTL signal with minimum pulse width of 11ns.

The user may disable some or all the channel trigger sources. A trigger source from any of the other channels can be selected where extern≥l trigger broadcast or synchronous acquisition of multiple channels is desired. When pulse overlapping happens due to closely spaced triggers, the user may choose to discard the second trigger or to store all pulses. In the last case the first pulse will be incomplete but will have a known number of samples.

2.3 BUFFERING BLOCK

Each acquisition channel has an independent buffering block which is organized in two stages designated as Pre-Trigger Buffer (PTB) and Secondary Buffer. The first stage is a free-running circular buffer with a read pointer that will stay behind the write pointer by a user defined value that corresponds to the number of pre-trigger samples. This number can have any value from 0 to 2046. The buffer data width is 8-bit and is filled at the data acquisition rate (200 MHz) being simultaneous written and read. The PTB pointers automatically recover from external induced errors such as electromagnetic interference or incident radiation, in a period no longer than 10.23μs.

The second stage of buffering is used for the temporary storage of pulses. The process is initiated by a trigger on the channel which automatically reserves the space required for a complete pulse on the SB followed by the storage of the user defined number of samples (from 8 to 2048 in multiples of eight) at 200MSamples/s (8-bit wide). The information about the reserved space is stored on PPR as part of the pulse parameters.

The SB data is read in real-time by the DSP in 64-bit words containing eight samples mapped from lower to upper byte at maximum peak rate of 800MByte/s and an expected sustained rate of 300Mbytes/s. This means that for pulses with 256 samples (1.28μs width) the maximum sustained aggregate hit rate (on all channels) is 1.17MPulse/s or 3.75MPulse/s while for 80 samples per pulse (0.4μs) it may reach 3.125MPulses/s and 10MPulses/s for sustained and peak rates, respectively, independently of the pulse source.

2.4 PULSE STAMPING

Each acquired pulse on any channel is tagged with the channel number from where it was generated, the mapping on the SB where it was temporarily stored and the time at which the trigger occurred. This information is stored in a circular buffer, the Pulse Parameter Recorder, with capacity for 512 tags, which can be read in real-time by the DSP. The time marks have a resolution of 5 ns and are given by a 40-bit counter, which is being incremented synchronously with the data acquisition clock. The counter can be started by software or by an external TTL pulse with minimum width of 11ns, allowing the synchronization of multiple boards.

2.5 DSP INTERFACE BLOCK

The DSP Interface Block (DSPIB) allows the DSP to access the FPGA registers, the Pulse Parameter Recorder and the Secondary Buffers. The DSPIB is composed of three blocks: the External Memory Interface Control (EMIC), the Interrupt Generation Block (IGB) and the Automatic Transfer Control (ATC).

The EMIC controls the read and write operations on the DSP to the FPGA internal registers and buffers. The EMIC complies with the Programmable Synchronous Interface of the DSP EMIFA [6] with no write latency and a three period latency for access of 64-bit words at the maximum rate of 100MHz.

The FPGA registers are 64-bit wide. Some of these are for read-only and provide information

about the FPGA internal logic while others are read/write registers used to store the configuration of the pulses, the triggers and the operational settings.

The IGB manages the request of interruptions to the DSP, initiating the real-time data transfers from the FPGA buffers to the SDRAM. The events which originate interruptions are the timer counter overflow or the SB when filled with the user defined number of pulses. These events may be mapped into any of the external DSP interruptions allowing, for instance, attributing higher priority interruptions to most frequent events.

The ATC manages the Peripheral Device Transfer (PDT) and the Single Port Access (SPA) modes that can be used by the DSP to achieve a higher sustained bandwidth, which may exceed 600 MByte/s (corresponding to 7.5-MPulses aggregate hit-rate at 80 samples/pulse) or free the CPU resources in the case of the Single Port Access modes. The increased performance may imply limitations on real-time activities like data processing or dynamic pulse parameter configuration.

2.6 DATA READOUT AND PROCESSING BLOCK

The data storing process is completely controlled by the DSP which can use several data transfer modes (Figure 5) depending on the application. Pulses are read by the DSP to its internal memory where they are processed or dispatched to the SDRAM, or written directly from the FPGA to the SDRAM using PDT transfer mode. The choice is dependent on the pulse rate, since intermediate storage in the DSP internal memory decreases the sustained pulse transfer rate to less than half of the available bandwidth (400Mbytes/s). This happens because the DSP originates two transfer operations for each word transferred. Figure 5 depicts the logical paths to and from the SDRAM: a) Direct storage using PDT (controlled by the DSP); b) Indirect storage using DSP internal memory; c) Storage with real-time data processing; d) DMA data readout by the PCI host. After the end of the acquisition process the host can retrieve the data stored on the SDRAM through the DSP PCI interface.

3. SOFTWARE

To demonstrate the module capabilities, a Graphical User Interface (GUI) test program was developed, which provides simple set-up of the module registers and graphically displays the acquired pulses. The program includes a device driver developed with the WinDriver™ tool from Jungo® [8]. Figure 6 shows the graphical appearance of the developed GUI: the top screen shows the set-up window; the bottom screen shows a graphical display of 10 pulses with 2000 samples each, where Y-axis represents the ADC binary value. Figure 6. Windows of the GUI test program.

CONCLUSIONS

A low-cost module has been implemented in a standard PCI card providing a flexible platform for application requiring multiple channel pulsed data acquisition where fast trigger algorithms can be implemented. Accurate time stamping and real-time processing is provided as well as a large memory pool. The direct attachment of the four input channels to the reconfigurable FPGA allows independent

operation and future implementations changes to provide extended capabilities. Preliminary tests confirmed the expectations that the module can achieve the high pulse rate which will be required by the MPRu diagnostic.

ACKNOWLEDGMENTS

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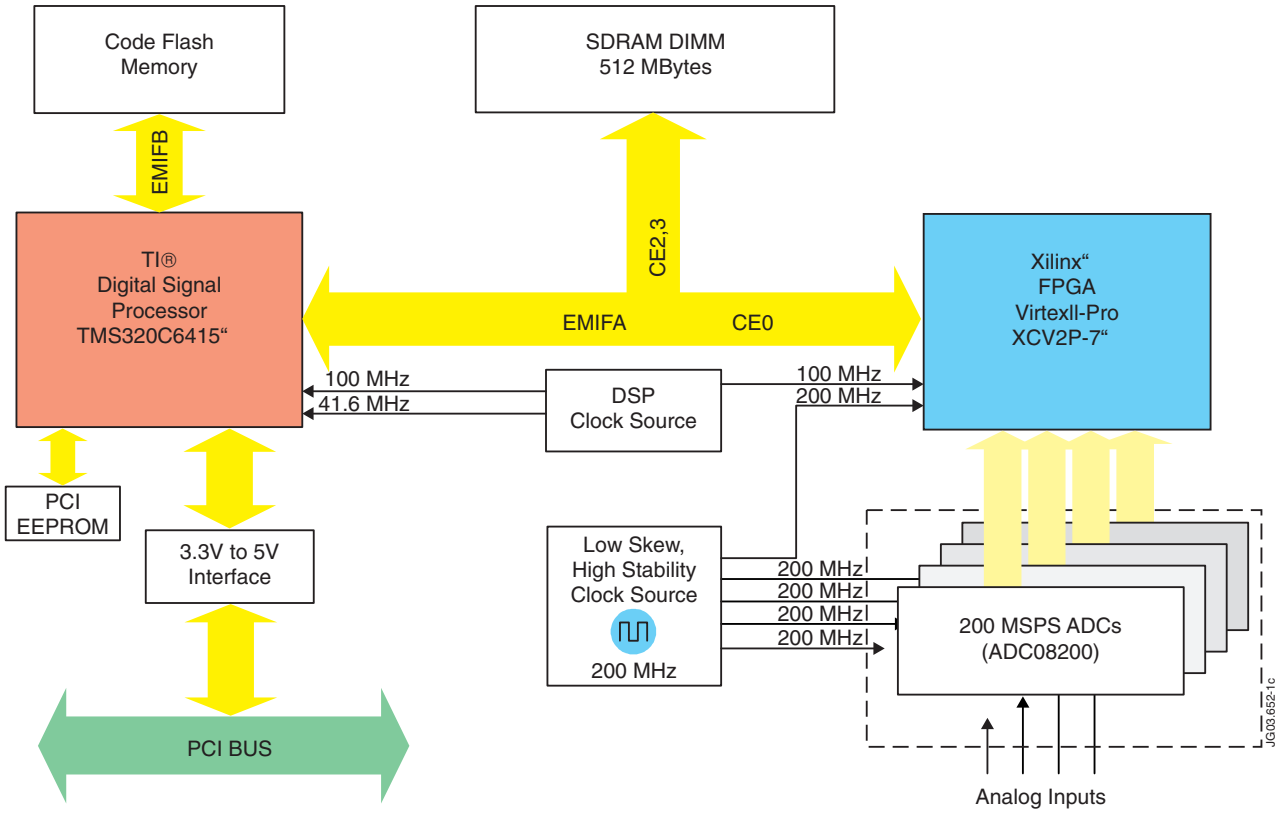

Figure 1: Module block diagram.

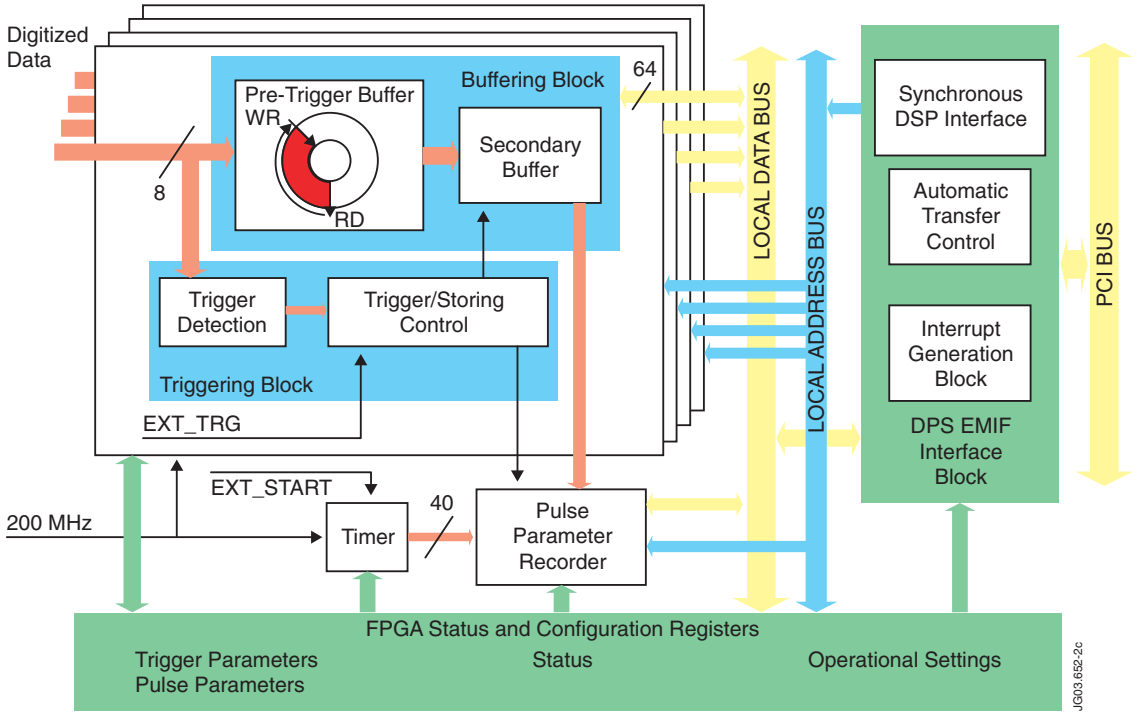

Figure 2: Block diagram of FPGA internal circuit.

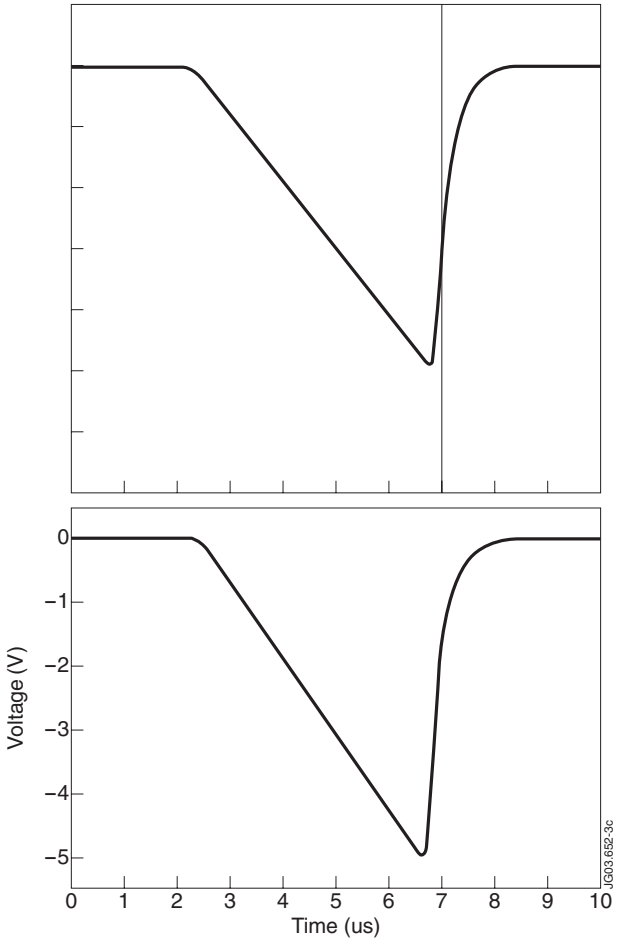

Figure 3: Comparison between acquired pulse data from a oscilloscope and by the transient recorder.

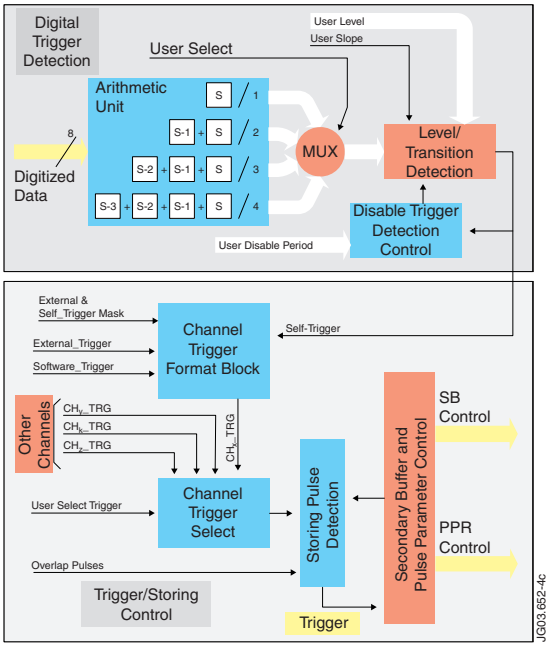

Figure 4: Trigger block diagram

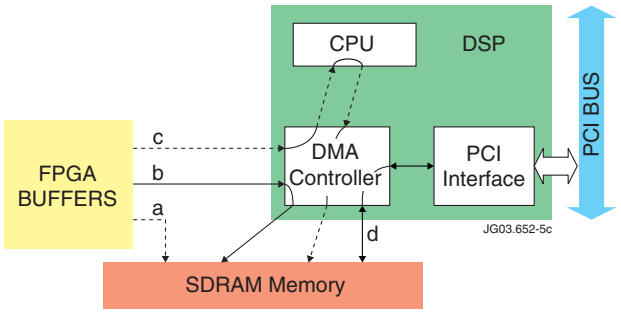

Figure 5: Logical paths to and from the SDRAM.

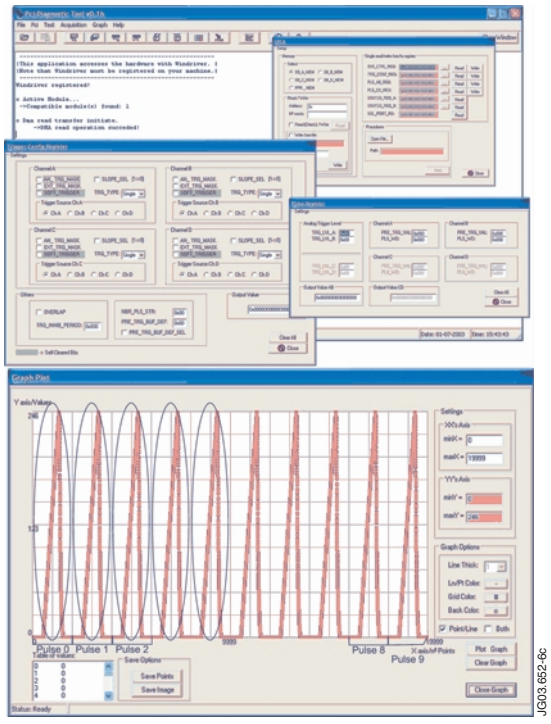

Figure 6: Windows of the GUI test program.