EUROPEAN FUSION DEVELOPMENT AGREEMENT

EFDA–JET–CP(03)02-1

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** See annex of J. Pamela et al, "Overview of Recent JET Results and Future Perspectives", Fusion Energy 2000 (Proc. 18th Int. Conf. Sorrento, 2000), IAEA, Vienna (2001).*

Preprint of Paper to be submitted for publication in Proceedings of the
4th IAEA Conference,
(San Diego, California, USA 21-23 July 2003)

ABSTRACT

A test-bench which generates the stimulus signals for testing a real-time control system and simultaneously recording its output variables is being developed for the JET real-time measurement and control tools. The system allows testing the operation of a real-time control system by using as inputs the plasma variables previously stored on the JET pulse database or user defined waveforms. This non-intrusive test method allows testing the control system for all possible operation scenarios in a faster duty-cycle without harming the machine to be controlled. The test-bench includes a 32 channels analogue stimulus generator and a 32 channels transient recorder device. The stimulus and recorded data are input to an MDSplus server and managed through a user interface elsewhere on a remote terminal over an Ethernet link. A HTTP server included on both signal generator and recorder devices allows to retrieve the signal names from previous JET pulses through the CODAS Level 1 interface, as well as the operation parameters (e.g. test pulse number, predefined waves selection, addition of noise, etc).

1. INTRODUCTION

The operation and scientific exploitation of a large fusion device such as the Joint European Torus (JET) have tight schedules which must not be affected by unstable ontest control systems that can be highly harmful and costly. New real-time control subsystems must be tested offline for all the possible operation scenarios regardless of its complexity and consequent testing difficulty. The proposed test-bench will permit to test offline the operation of a real-time control sub-system without affecting the machine. It will simulate the JET signal environment, allowing systems to be more thoroughly tested before they go on-line on the JET machine. Consequently development and maintenance times should reduce, system performance and reliability should improve.

The system under test (SUT) is viewed as a black box to which stimulus signals are input and output signals are analyzed to evaluate the operation. User defined signals or the plasma signals previously stored on the JET pulse database can be used as stimulus for the inputs.

Figure 1 presents the test-bench which is based on a Real-Time Signal Generator (RTSG) device and on a Real-Time Signal Recorder (RTSR) device. Both RTSG and RTSR have enough memory to source the analogue output signals on all channels for a total time of at least 15 seconds, at 1 Mega Samples per Second (MSPS), with no data repetition. Real-time data decompression can be implemented in the reprogrammable logic to augment the total signal sourcing period. Programmable time marks supplied by the JET Composite Timing and Triggering System (CTTS) [1] permit to define signal sourcing intervals in a broader operation period. Real-time reloading of analogue signal vectors to the RTSG outputs is possible but duty-cycle is dependent of the database access bandwidth. Lower output data rates can be attained by interpolating the lower rate data on an up-sampling fitter module before the output buffers. This process can be implemented in the reprogrammable hardware to alleviate the processor and to avoid reprogramming the output reconstruction filter, which will remain with a fixed frequency bandwidth thereby being easier to implement.

Stimulus and recorded data are contained in a Model Data System plus (MDSplus) [2,3] server and managed through a user interface elsewhere on a remote terminal over the Ethernet network. Signal names from previous JET pulses are obtained through the Control and Data Acquisition System (CODAS) Level 1 interface [4] through a Hypertext Transfer Protocol (HTTP) server [5] included on the RTSG. The same HTTP server is used to setup both RTSG and RTSR with its operation parameters like test pulse number, predefined wave selection, addition of noise, etc.

The RTSG provides up to 32 analogue output channels to generate the stimulus for the SUT. Additionally the stimulus data can be transmitted through an Asynchronous Transfer Mode (ATM) link to the JET real-time measurements and control processors which have this type of interface [6,7,8]. Up to 32 analogue output or ATM networked signals from the SUT can be recorded by the RTSR for later analysis. Both devices may optionally be interconnected, through standard Multi-Gigabit point-to-point links, to expand the total number of channels or to optionally implement a gateway between the existing ATM/Ethernet links and other high-speed serial communications protocols.

The CTTS optical network will be used to synchronize the RTSG and the RTSR with the SUT.

2. HARDWARE

The RTSG and RTSR have the same hardware platform, except for the modular analogue IO, and are based in a System-on-a-Chip (SoC) architecture, centred on the Xilinx® Virtex-II Pro™ XC2VP20-6FF896 Field Programmable Gate Array (FPGA) [9]. This FPGA includes 2 embedded 350 MHz PowerPC 405™ (PPC) Reduced Instruction Set Computers (RISC) processors and eight Multi-Gigabit transceivers for low-latency high-speed serial communications like Peripheral Component Interconnect Express (PCI Express) and others.

Both RTSG and RTSR contains up to 1 GByte of DDR Double Data Rate Synchronous Dynamic Random Access Memory (SDRAM) memory in Small Outline Dual Inline Memory Module (SODIMM) format, up to 1GByte CompactFLASH memory, a 10/100MBits/s Ethernet RJ-45 port, an ATM OC-3 (155Mbit/s) PCI Mezzanine Card (PMC) interface with a dual SC optical link and the CTTS interface.

The RTSG (Fig.2) output channels generate analogue signals synchronously at the rate of 1MSPS. Each channel contains a 12-bit (optionally up to 16-bit) resolution Digital to Analogue Converter (DAC) and a fixed bandwidth signal reconstruction filter with an output range of +/-10V.

The RTSR (Fig.2) analogue input channels are simultaneously sampled at the rate of 1MSPS and have settable gain. Each channel contains an Analogue-to-Digital Converter (ADC) of 12-bit resolution, upgradeable to 16-bit, and a fixed bandwidth anti-aliasing filter with an input range of +/-10V.

Due to the common hardware architecture, the RTSG and the RTSR can be merged into one hybrid device having the following configurations: 24 analogue outputs + 8 analogue inputs, 16 analogue outputs + 16 analogue inputs, 8 analogue outputs + 24 analogue inputs.

Both devices are modular and enclosed in a 19”, 1U form factor case (Figure 3), which is easily

transportable and can be fitted in a standard 19” rack. Each I/O analogue channel is provided on a front panel LEMO® plug.

3. FIRMWARE

The FPGA firmware development of the test-bench is based on the Coreconnect™ bus from IBM® and on the VERILOG language [10]. The PowerPC processor (PPC) processor peripherals e. g. timers, DDR SDRAM controller, FLASH memory controller, Ethernet interface, ADC/DAC interface, Timing Unit, CTTS interface, Multi-Gigabit serial communications interface and the PPCs are interconnected by the FPGA internal Coreconnect™ bus. The ATM interface connects to this bus through a PCI bridge.

Figure 4 presents the FPGA firmware architecture where one of the PPCs is dedicated to the Multi-Gigabit point-to-point communications and the other one to the remaining controllers and interfaces mentioned above. This topology can be reconfigured in order to maximize the processing power efficiency of both processors. This may happen if only one PPC is not enough to process the algorithms of stimulus generation. Then the second PPC can be used to perform this task.
CORECONNECT PLB 1 PowerPC

The ADC/DAC serial interface is based on a Dual Port RAM (DPR) memory to implement the ADC/DAC data buffer and a serial decoder/encoder block. A sample rate converter, to obtain lower acquisition/generation data rates, is incorporated between the ADC/DAC data buffer and the processor bus.

The address bus of the DPR is driven by the Timing Unit time counter thus providing the time stamping of the sampled data in the case of the ADCs and the output data time mark in the case of the DACs. The time counter is incremented by a frequency derived from the JET CTTS timing system through an external Phase Locked Loop PLL.

The FPGA and the ADC/DAC blocks are linked through serial interfaces which allow reducing the number of interconnection signals. This approach also permits implementing digital galvanic isolation if desired.

4. SOFTWARE

The test-bench will be controlled by a test supervisor CODAS subsystem which uses the following programs: the General Acquisition Program (GAP) which performs the prepulse checks, initialization and post-pulse data collection, the GAP tree editor, the Countdown touch panel (cdutil) which sends the initialization messages to the systemunder- test and the pulse schedule editor (xspedit) which prepares the test session pulse schedules in advance.

The test-bench embedded software includes the HTTP server and Common Gateway Interface (CGI)* scripts which communicates with the Level 1 interface of the test supervisory subsystem, the DAC/ADC device driver, the ATM controller and the client to the MDSplus server database.

The Ethernet and ATM device drivers besides a CompactFLASH booting process are provided

* http://hoohoo.ncsa.uiuc.edu/cgi/intro.html.

by the Linux® [11] for PPC operating system ported by DENX** which also includes support for real-time.

CONCLUSIONS

The proposed test-bench will provide a signal generator and recorder to test new realtime measurement and control tools. It allows testing the functionality, performance and the response to abnormal inputs of the system-under-test. Additionally, it will improve the test rate without having the safety issues associated with online control.

The reconfigurable SoC approach used for the hardware is cost effective and permits reconfiguring/debug the system without resorting to costly hardware modifications. The test-bench will be integrated in CODAS and run as a JET test-pulse. An MDSplus server, which is becoming a de facto standard for fusion, is used for storing the stimulus vectors and acquired data allowing the operation of the system without taking bandwidth from the JET pulse database.

ACKNOWLEDGEMENTS

The Real Time Project is a JET real-time measurement and control tools enhancement within the EFDA-JET work programme performed as a EURATOM collaboration between IST, CEA and UKAEA/JET. This work has been carried out within the framework of the European Fusion Development Task Agreement (Contract JW3-TAEP-RTP-01), with financial support from the European Communities and the JET joint fund. The views and opinions expressed herein do not necessarily reflect those of the European Commission and the EFDA Associates.

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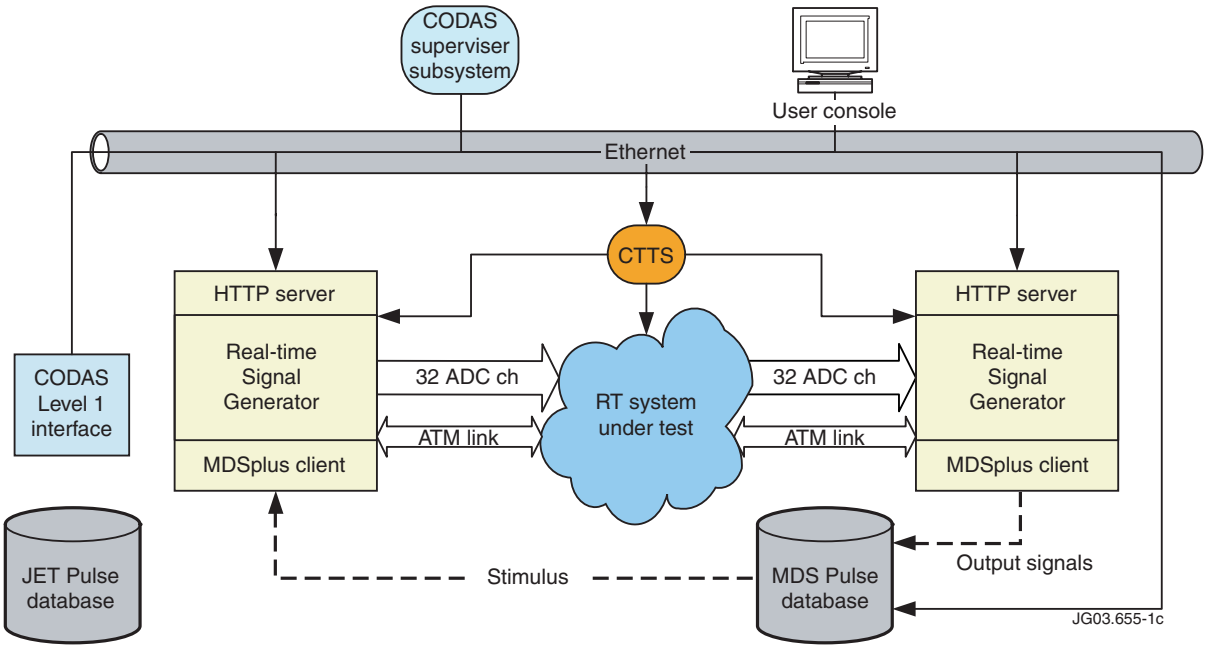

Figure 1: Global test-bench architecture.

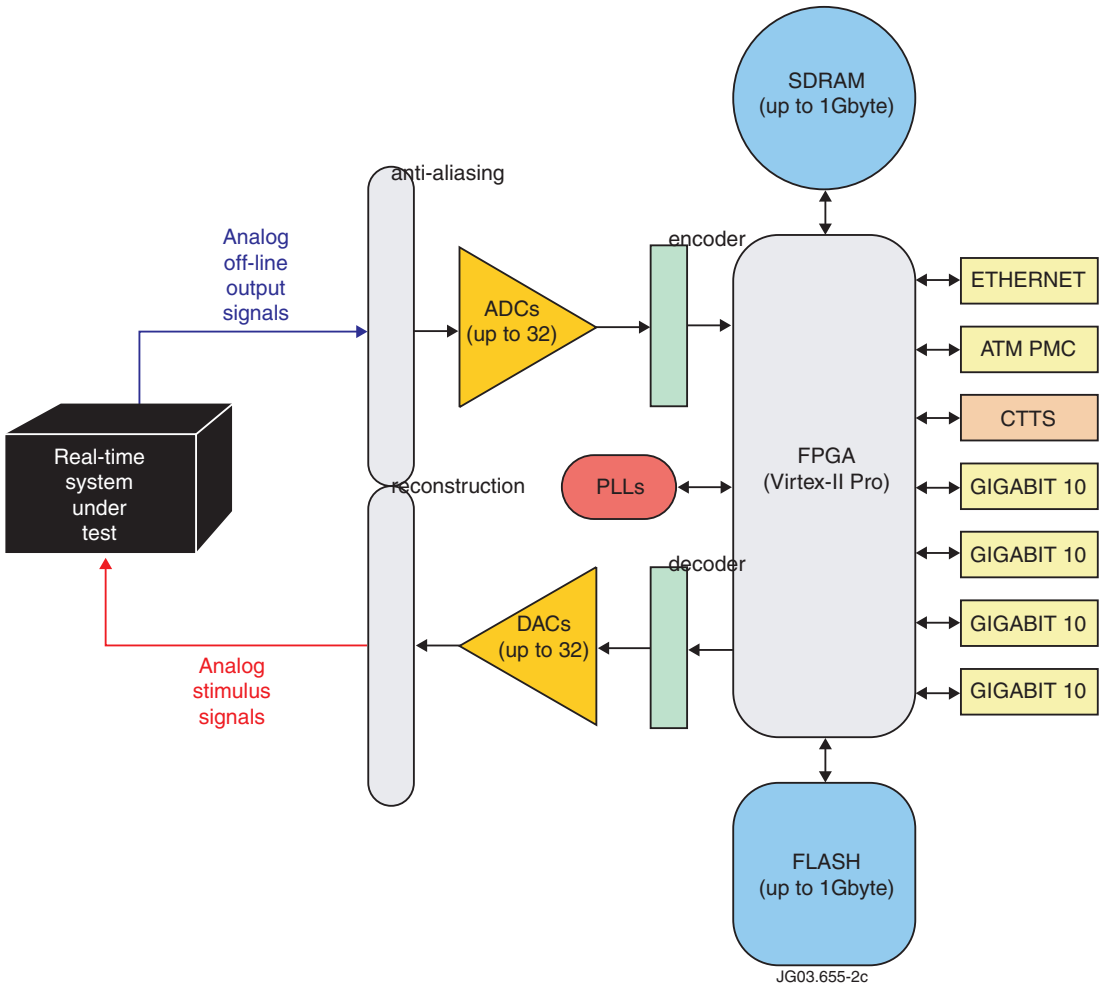

Figure 2: RTSG and RTSR devices architecture

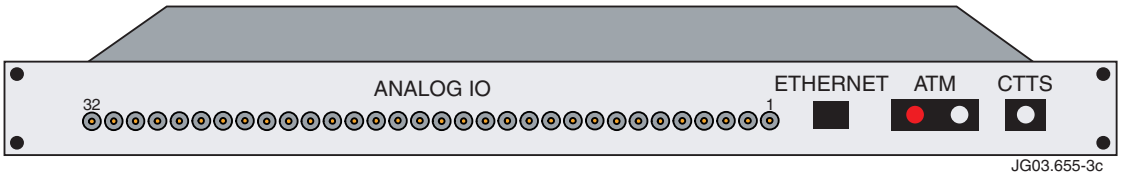

Figure 3: RTSG and RTSR devices case and front panel view.

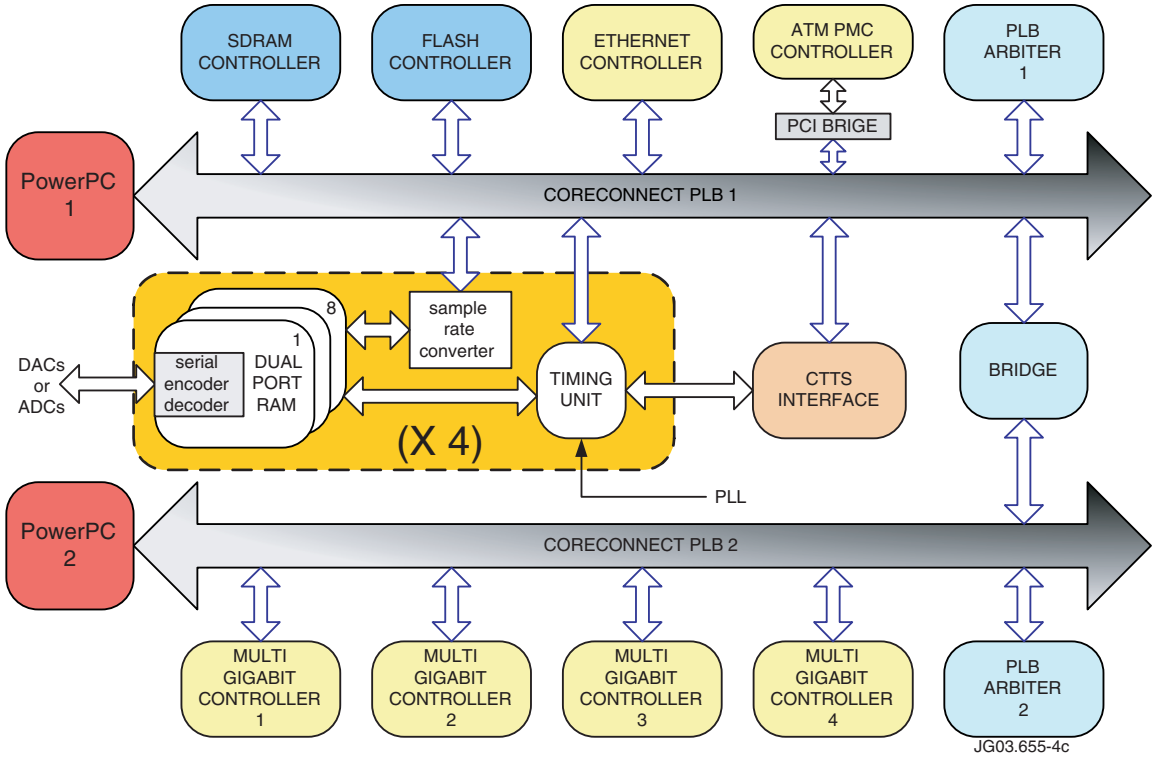

Figure 4: FPGA architecture.